

**HMC424LP3 Negative Biased
Digital Attenuator TTL/CMOS Driver Circuit Design**

General Description

The HMC424LP3 is a broadband 6-bit GaAs IC digital attenuator in a low cost leadless surface mount package. The attenuator covers a frequency range from DC to 13 GHz with a typical insertion loss of less than 4 dB. Major attenuation steps are 0.5(LSB), 1, 2, 4, 8, and 16 dB with total attenuation of 31.5 dB. Attenuation accuracy is excellent at ± 0.5 dB typical step error with an IIP3 of +32 dBm. A single Vee bias of -5V allows operation at frequencies down to DC while six control voltage inputs, toggled between 0 and -5V, are used to select each attenuation state.

Introduction

Negative biased digital attenuators have the advantage of operation over wide RF bandwidths and excellent attenuation accuracy down to DC. Conversely, positive biased digital attenuators have a low frequency limit imposed by the on-chip-capacitors used for RF grounding. Therefore a negative biased attenuator is preferred in applications requiring operation to very low frequency. In order to switch between attenuation states, the user must apply negative control voltages to the control input pins. Since control signals generated by common logic families are positive voltages, a driver circuit capable of translating these logic level signals to inputs compatible with the digital attenuator is required. In addition, the number of components needed to realize the driver circuit and the space required to implement the circuit on the PCB must be minimized to control manufacturing costs.

Attenuator Operation

The HMC424LP3, a negative bias digital attenuator, is realized as a cascade of switches and fixed attenuator pads as shown in the functional diagram of figure 1. The attenuation is set by adjusting each of the control pins (V1 – V6) to either a logic “high” or logic “low” per table 1. The input control voltages must be within the range specified in table 2 in order to operate the attenuator as specified. To operate this device from standard logic families, a driver circuit has been designed that interfaces TTL/CMOS logic to the HMC424LP3.

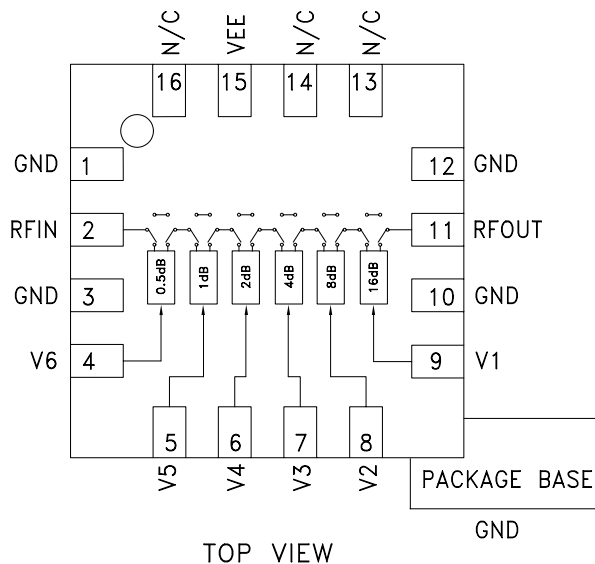


Figure 1 – HMC424LP3 functional diagram

Control Voltage Input						Attenuation State RF1 - RF2
V1 16 dB	V2 8 dB	V3 4 dB	V4 2 dB	V5 1 dB	V6 0.5 dB	
Low	Low	Low	Low	Low	Low	Reference I.L.
Low	Low	Low	Low	Low	High	0.5 dB
Low	Low	Low	Low	High	Low	1 dB
Low	Low	Low	High	Low	Low	2 dB
Low	Low	High	Low	Low	Low	4 dB
Low	High	Low	Low	Low	Low	8 dB
High	Low	Low	Low	Low	Low	16 dB
High	High	High	High	High	High	31.5 dB

Any Combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.

Table 1 – HMC424LP3 truth table

State	Bias Condition
Low	0 to -3V @ 70 μ A Typ.
High	-5 to -4.2V @ 5 μ A Typ.

Table 2 – HMC424LP3 control voltages at Vee = -5V

Driver Circuit Design

The driver circuit to interface TTL/CMOS to the digital attenuator is shown in figure 2. This circuit is duplicated for each control line, resulting in a total of six circuits for the HMC424LP3 digital attenuator.

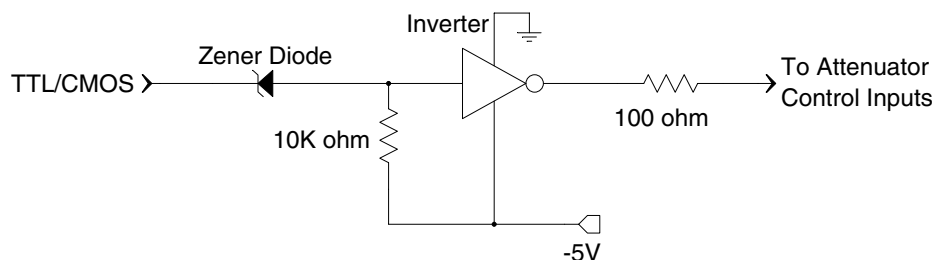


Figure 2 – Driver circuit schematic

The driver circuit converts the output signals from the TTL/CMOS devices to 0V and -5V respectively for the inputs of the HMC424LP3. In figure 2, the zener diode is used to level-shift the TTL/CMOS outputs down by the zener voltage V_z . The standard zener voltage for commercially available zener diodes in this

range is -5.1V. The inverter logic gate is biased with 0V at the Vcc pin by grounding this pin and -5V at the ground terminal to operate the logic gate with negative voltage. Finally, a 100 ohm series resistance is added to minimize RF leakage between control pins.

The input-output characteristic of the TTL/CMOS driver circuit is shown in figure 3 while a summary of the voltages at different nodes of driver circuit is shown figure 4.

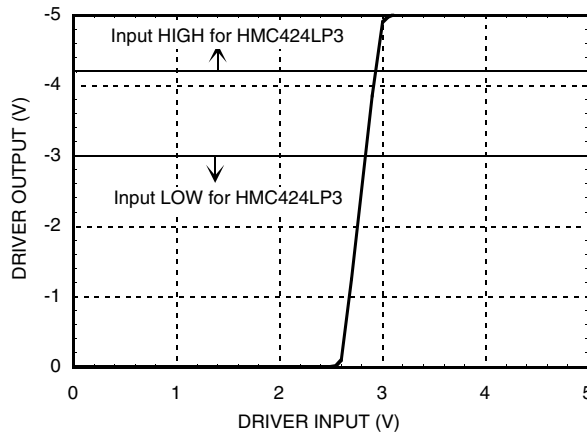
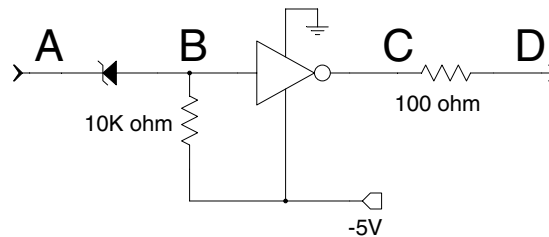


Figure 3 – Input-Output Characteristic of Driver Circuit



A TTL/CMOS Output Signal	B Input of the Inverter	C Output of the Inverter	D Control Input of HMC424LP3
LOW (0 to +0.5V)	-5V	0V	LOW
HIGH (+2.5V to +5V)	0V	-5V	HIGH

Figure 4 – Summary of voltage levels

Since one driver circuit is required for each control input of the attenuator, figure 2 is duplicated six times to create the complete schematic of the driver and attenuator shown in figure 5. In order to realize the circuit of figure 5 in a minimum PCB design area, integration of the circuit elements was a major design criterion. Circuit elements were obtained in an array format including the hex inverter array, the recently-developed zener diode array¹ and the 10kΩ resistor array.

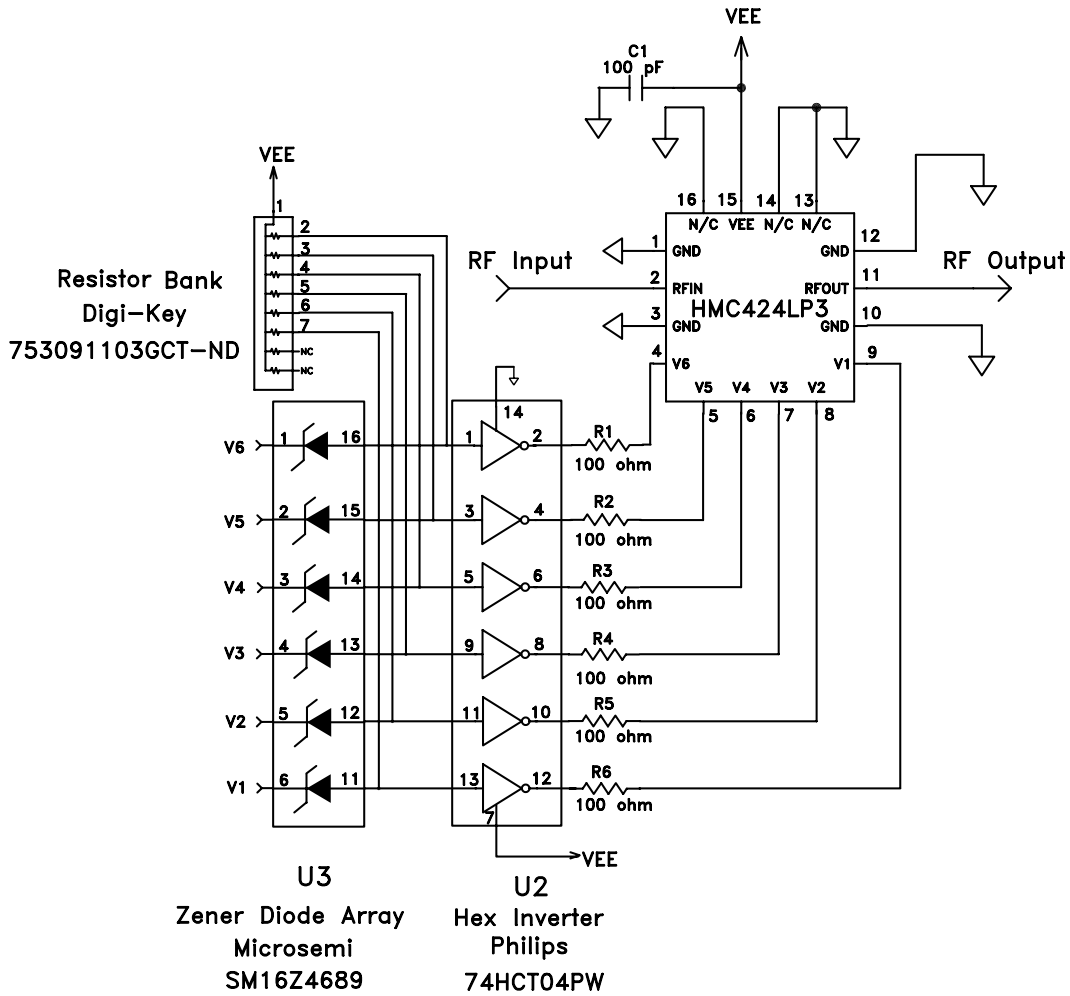


Figure 5 – Complete driver schematic

Driver Circuit Layout

Figure 6 shows the physical layout of the application circuit board for HMC424LP3 with the driver circuit. The board material is Rogers 4350 with a total thickness of 10 mils, selected to achieve good RF performance through 15 GHz. Coplanar lines are utilized to minimize radiation from the RF traces and to minimize their width. C1 is a bypass capacitor added to minimize bias voltage noise and ripple from the external supplies. U2 is the hex inverter and U3 is the zener diode array.

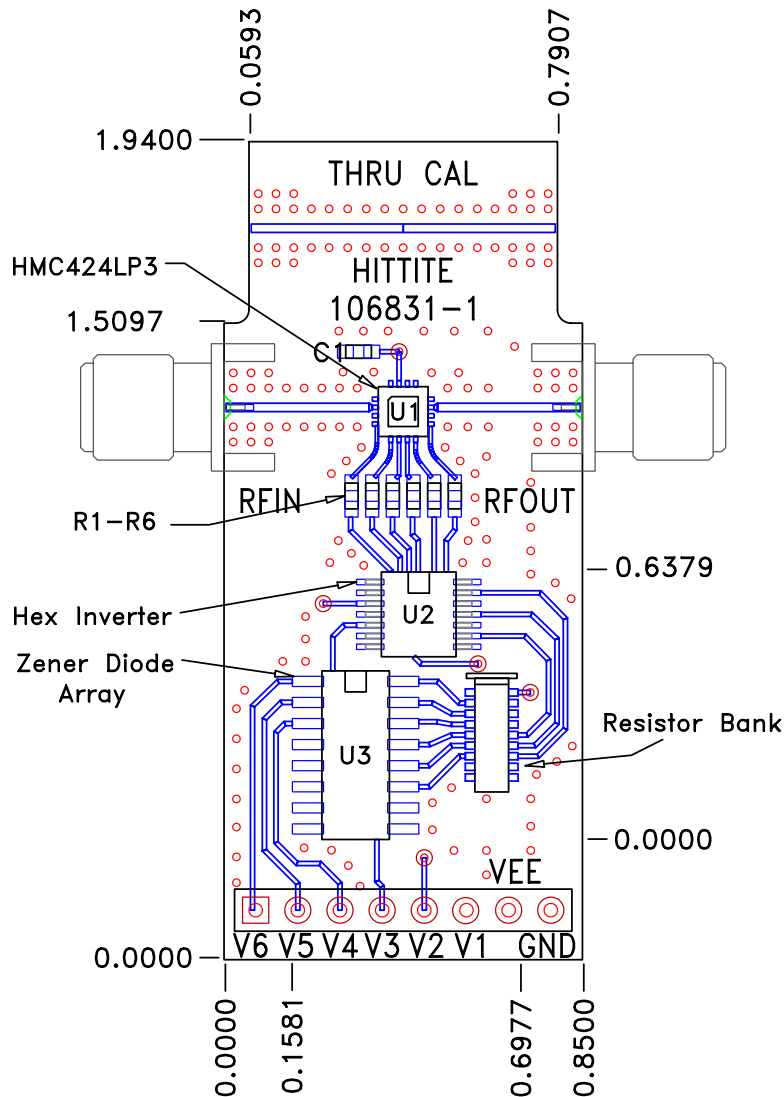


Figure 6 – HMC424LP3 evaluation board with driver circuit

Circuit Performance

Since the digital attenuator is being supplied with its specified control voltage levels and there is no change to the RF circuit, there is no degradation in RF performance of the HMC424LP3. Full attenuation range and accuracy is maintained over the entire operating frequency range as shown in figure 7. Moreover, with the use of high speed CMOS inverter technology with very low current consumption, the driver circuit adds only one gate delay to the settling time and switching speed.

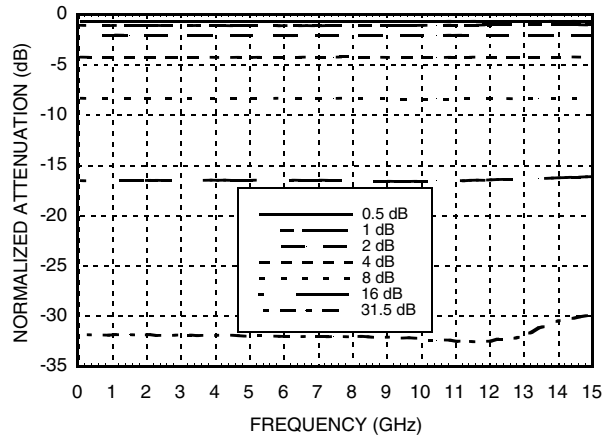


Figure 7 – HMC424LP3 normalized attenuation

Conclusion

This product note has detailed the design, layout and performance of a driver circuit interfacing the HMC424LP3 digital attenuator to TTL/CMOS outputs in a minimum board space. The driver circuit does not limit the RF performance of the attenuator or appreciably degrade switching speed. This circuit topology can be utilized to drive a wide variety of negative bias switch and attenuator products available from Hittite Microwave Corporation including the HMC307QS16G and HMC335G16 5-bit digital attenuators, the HMC344LP3 SP4T and the HMC322LP4 SP8T.

(Endnotes)

¹ For a complete description of this product please contact Microsemi Corporation or visit www.microsemi.com

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HMC424LP3 PRODUCT NOTE

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