

FREQUENCY DIVIDER OPERATION & COMPENSATION WITH NO INPUT SIGNAL

Frequency Divider Operation & Compensation With No Input Signal

General Description

The Hittite Microwave pre-scalar product line consists of over 20 low noise, static dividers utilizing InGaP HBT technology that accept a broad range of input signals, from DC (with a square wave input) through 18 GHz microwave frequencies. Division ratios of 2, 3, 4, 5 and 8 are available along with +3V and +5V single supply versions. All divider products exhibit very low additive SSB phase noise with the best products delivering -153 dBc/Hz at 100 kHz offset, enabling synthesizer designers to maintain excellent system noise performance. This application circuit discusses how to prevent self-oscillation and subsequent “false triggers” in the dividers when no RF power is presented at the device input.

Application Problem

Dividers are used in a wide variety of applications ranging from consumer electronics to military and satellite systems. Specifically, dividers are incorporated in circuits such as phase locked loops or synthesizers. In each of these applications the RF signal is continuously incident on the input of the frequency divider presenting it with a constant dominant signal (S/N ratio high). However, other applications may not present a continuous RF signal to the input therefore leaving the input vulnerable to noise (S/N ratio low). One such application is a signal detection circuit shown in figure 1. This circuit detects the presence of RF energy by directly down converting through multiple divider circuits and performing an analog to digital transformation. The signal detection circuitry determines the frequency and then outputs the appropriate response.

When no input is present, the inputs to the dividers will be subjected to noise. Since the dividers are designed for maximum sensitivity, the input stages have a tendency to “self oscillate” with no or low signal input levels. This “self oscillation” tendency also causes the dividers to malfunction when the input signal slew rate is too low, such as with low frequency sine waves. Because the divider network is essentially “digital” in nature, any signal with a sufficient level will trigger a gate within the divider. If this occurs, the divider will produce an output due to this “false trigger”. This output will appear as multiple tones when viewed on a spectrum analyzer. The tones will be detected by the signal detection circuitry causing a false output to occur.

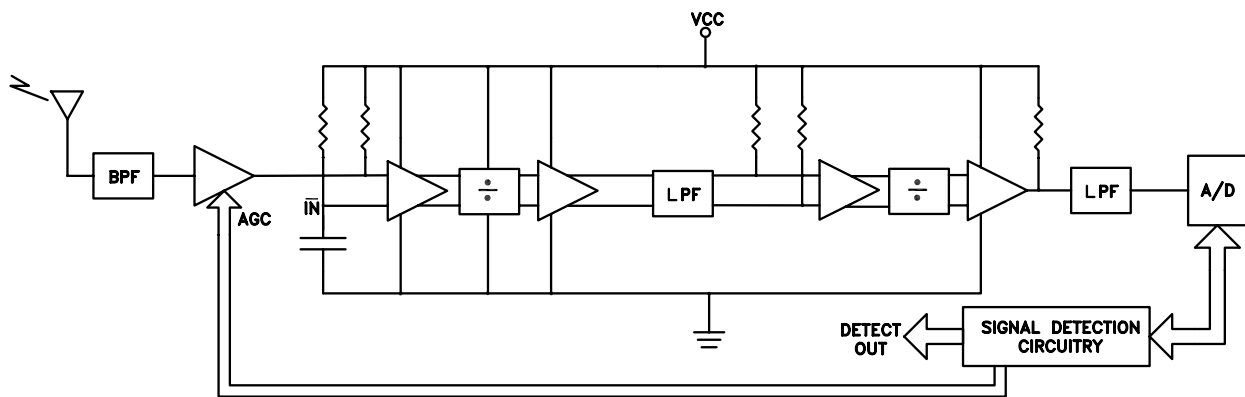


Figure 1 – Signal detection circuit

Therefore, it is essential to prevent the divider from false triggering in the absence of an RF signal. To prevent this condition, an offset voltage is applied across the inputs of the dividers to prevent the self-oscillation and therefore the false triggering of the divider in the absence of a signal.

Application Solution

Figure 2 shows a functional block diagram of a typical divider circuit. The circuit consists of three main components, a differential amplifier at the input, one or more digital divider networks, and an output differential amplifier. The input differential amplifier creates “digital like” output which, depending on the voltage levels,

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will trigger gates in the digital divider networks. The output differential amplifier receives the digital output and amplifies it accordingly. The input/output differential amplifiers have pull up resistors R1 to R4 (on chip) connected to Vcc. Capacitor C1 is external, and ties the complimentary input to RF ground for single ended input operation. Since the resistances R1 and R2 are equal, the difference in potential across the input terminals is zero when no RF is present. When the amplifier is in this state, any noise present at the input will be amplified and cause the digital divider to false trigger. However, when a nominal value of RF power is present at the input port, current draw through R2 creates a voltage drop across R2, resulting in a potential difference across the input terminals. In this state, the noise is suppressed and the false triggering prevented.

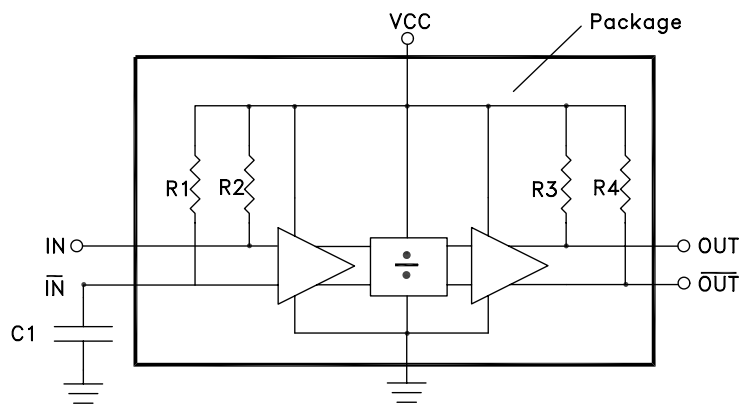


Figure 2 – Block diagram of typical frequency divider

By placing a resistor from the complimentary input port to ground, a potential difference is established across the input ports therefore preventing false triggering of the divider when no RF is applied.

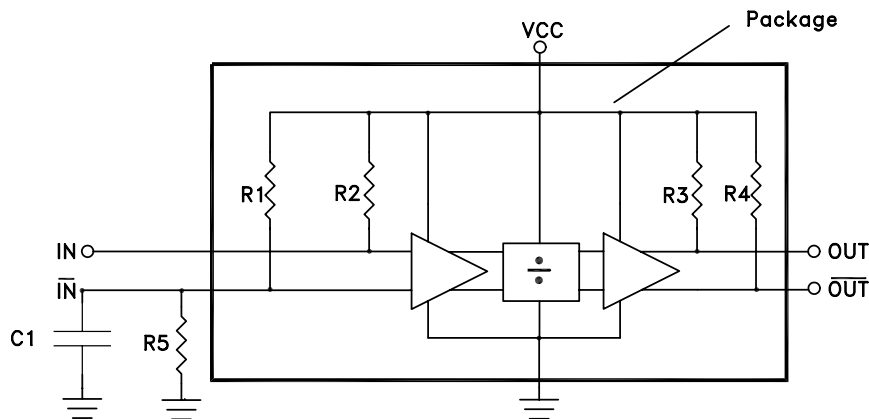


Figure 3 – Block diagram of typical frequency divider with offset voltage compensation.

Figure 3 is a schematic of a typical divider with offset resistor R5 placed at the complimentary input port. The value of the resistance is initially chosen to allow for approximately a 25 mV voltage differential between the input terminals but may be higher depending on the divider used. The resistor should be placed as physically close to the pin as possible to minimize parasitics.

Offset resistors were placed at the inputs of all of Hittite's dividers, checked over temperature (-40C to 85C) with, and without, RF applied. Figure 4 shows a typical evaluation board configured with offset resistor R5.

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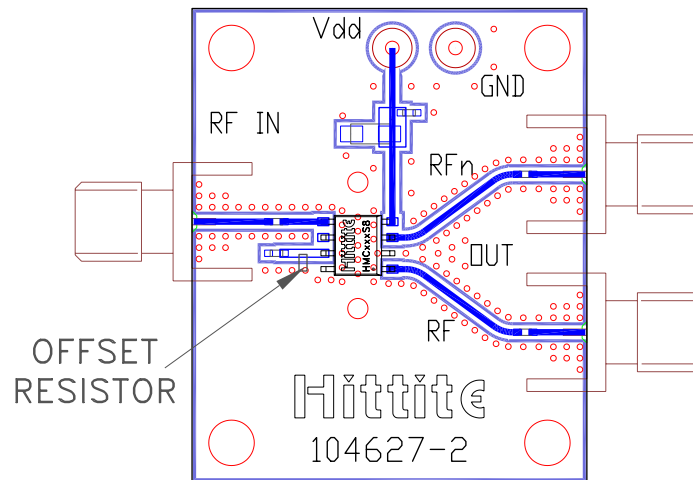


Figure 4 – HMC362 evaluation board with offset resistance

Figures 5A and 5B show plots of the spectrum, at the output of the HMC362S8G divider, from D.C. to 20GHz. Figure 5A shows the output spectrum when no RF is applied and with no offset resistor at the complimentary input. The multi-tone output is due to the “false triggering” of the digital divider. Figure 5B shows the spectrum under the same conditions but with an offset resistor at the complimentary input. The divider produces no output over the temperature range of -40C to 85C .

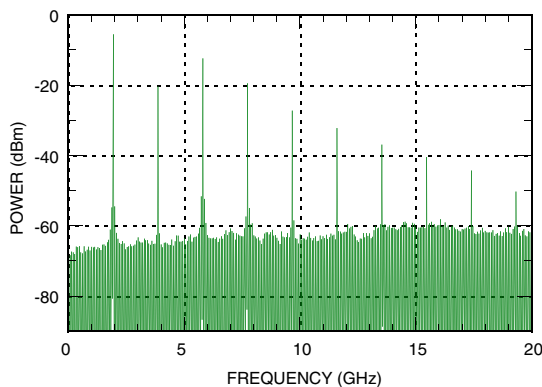


Figure 5A – Divider output with no input, and no offset resistance

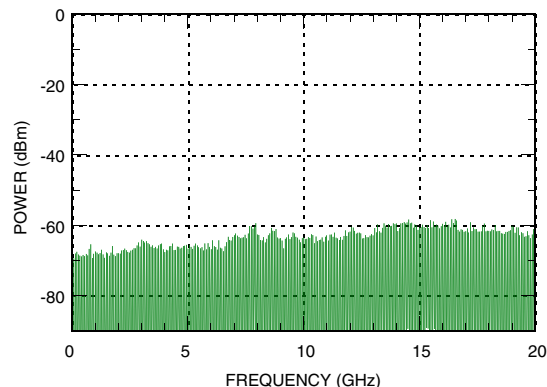


Figure 5B – Divider output with 40k Ω offset resistance

The majority of Hittite dividers have differential inputs/ outputs. However, three dividers are designed with single ended inputs/outputs. The exceptions are the HMC432, HMC433, and HMC434. Although these parts have single ended inputs, they still require offset resistances because internally the inputs are differential but have been terminated for single ended operation.

Limitations and Trade-offs

Due to the offset voltage created by the offset resistor, the input sensitivity of the divider will be affected. Figure 6 shows a plot of the input sensitivity with and without the offset resistor. The dotted line outlines the lower range of the input sensitivity of the divider with no offset resistor. The maximum input power is marked by the solid line.

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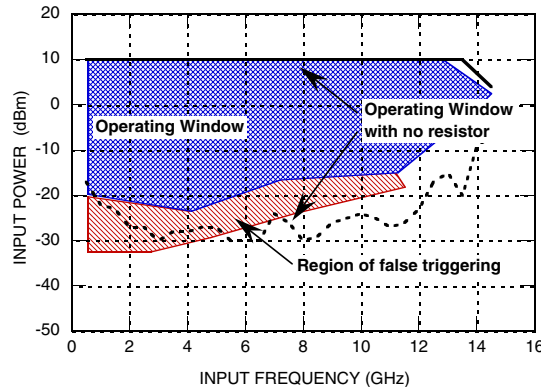


Figure 6 – Input sensitivity of the HMC362S8G with offset resistor

When an offset resistor is used, the minimum input power required for proper operation is higher as outlined by the lower boundary of double hatched area. The upper boundary of the double-hatched area is the maximum allowable input power.

Although the divider produces no output when no RF power applied, there will still be a region where the divider can false trigger. This area is marked by the single hatched area. In this region, the voltage differential across the input goes to zero (or close to it) due to the increased input signal. With increasing input power the voltage differential across the input is re-established and the divider operates normally.

Conclusion

HMC dividers provide exceptional reliability and performance in a variety of systems. In the majority of systems, these dividers require no special biasing. However, there are systems in which the dividers may “false trigger”. This normally occurs in systems where the input of the divider experiences periods where no RF power is present at the input. During these periods, the divider may produce “false triggers” due to noise present at the input. This can be prevented by applying an offset voltage across the input. This offset voltage is created by simply placing a shunt resistor from the complimentary input to ground.

Table 1 shows the recommended values of offset resistors for all of Hittite’s dividers over the temperature range of –40C to 85C. Appendix A shows the input power sensitivity plots for all the dividers, with and without offset resistors.

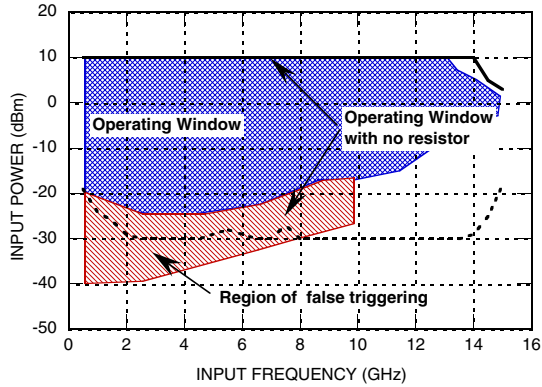
Divider Part Number	Offset Resistance (Ω)	Comments
HMC361S8G	40k	Offset resistor from pin 7 to ground
HMC362S8G	40k	Offset resistor from pin 7 to ground
HMC432	4k	Offset resistor from pin 3 to ground
HMC433	4k	Offset resistor from pin 3 to ground
HMC434	4k	Offset resistor from pin 3 to ground
HMC437MS8G	NONE	Offset resistor from pin 3 to ground
HMC438MS8G	NONE	Offset resistor from pin 3 to ground
HMC363S8G	60k	Offset resistor from pin 7 to ground
HMC364S8G	60k	Offset resistor from pin 7 to ground

Table 1 – Offset resistances for Hittite’s dividers

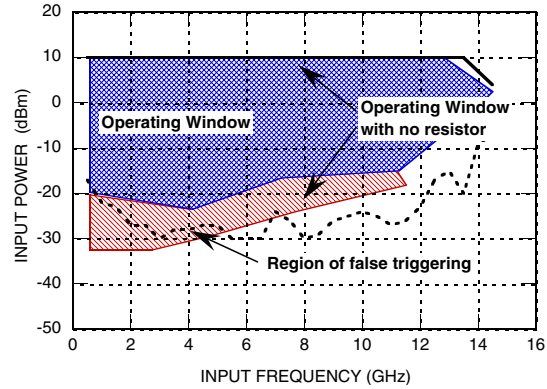
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Appendix A

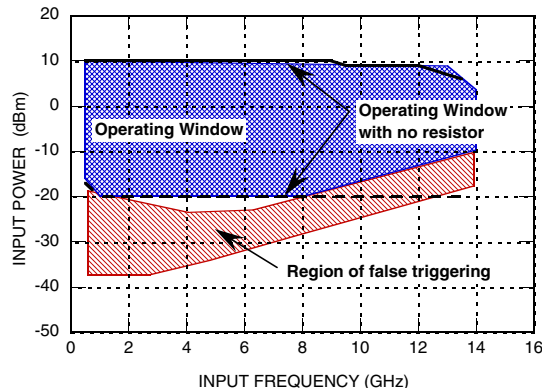
HMC361S8G Input Sensitivity & Operation, R= 40k Ω



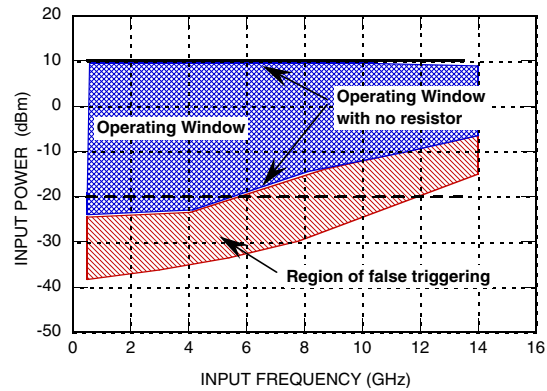
HMC362S8G Input Sensitivity & Operation, R= 40k Ω



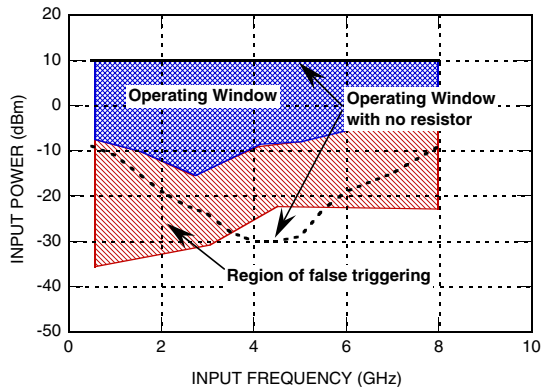
HMC363S8G Input Sensitivity & Operation, R= 60k Ω



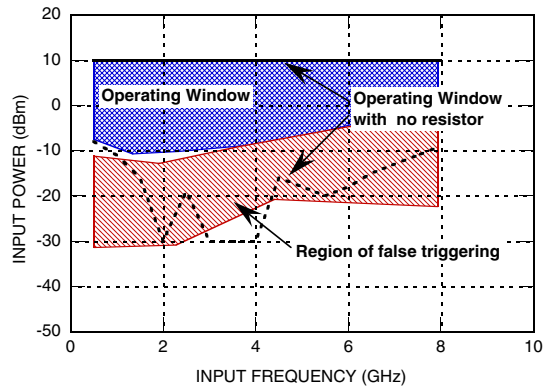
HMC364S8G Input Sensitivity & Operation, R= 60k Ω



HMC432 Input Sensitivity & Operation, R= 4k Ω

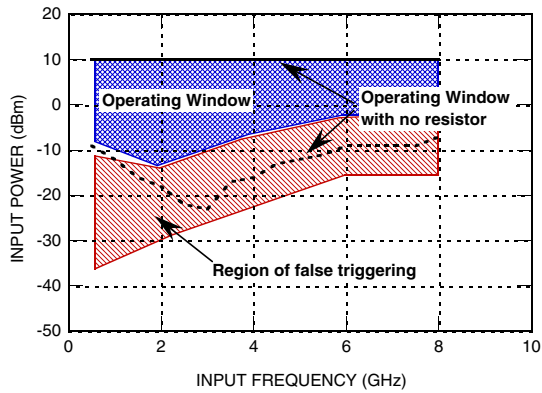


HMC433 Input Sensitivity & Operation, R= 4k Ω

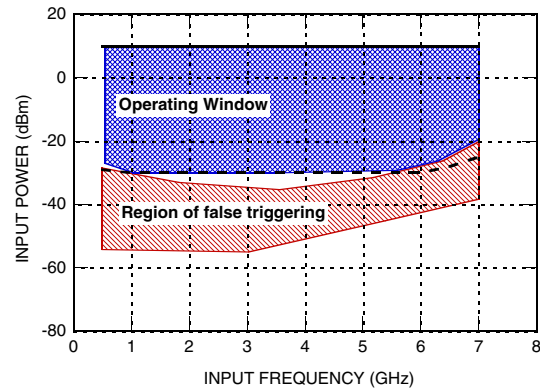


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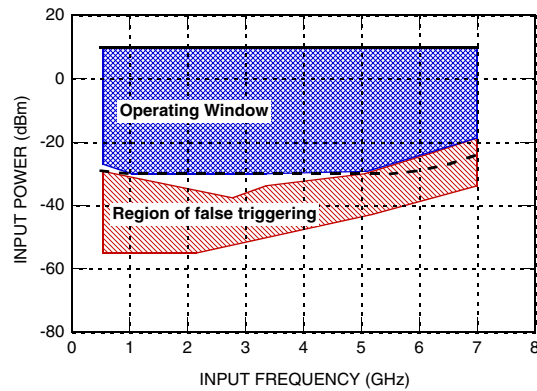
HMC434 Input Sensitivity & Operation, R= 4k Ω



HMC437MS8G Input Sensitivity & Operation, R= None



HMC438MS8G Input Sensitivity & Operation, R= None



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Notes: