

Extending the HMC189MS8 Passive Frequency Doubler Operating Range with External Matching

General Description

The HMC189MS8 is a miniature passive frequency doubler in a plastic 8-lead MSOP package. The doubler converts signals in the 2-4 GHz range at its input to an output frequency in the 4-8 GHz range. The suppression of undesired fundamental and higher order harmonics is 33 dB typical with respect to input signal levels. The doubler uses the same diode/balun technology used in Hittite MMIC mixers. The doubler is ideal for high volume applications where frequency doubling is more economical than direct higher frequency generation. The passive Schottky diode doubler technology contributes no measurable additive phase noise onto the multiplied signal.

Introduction

Wireless communications applications are constantly striving to put more functionality into smaller packages in order to reduce cost. An example of this is the Local Oscillator (LO) generation chain within a microwave radio (see Figure 1). In figure 1, the LO generation chain consists of a low noise frequency generator followed by frequency multiplication, amplification and filtering. Phase Locked Loop (PLL) circuits implemented with dielectric resonator oscillators (DRO's) or high frequency fundamental VCO's are typically used as the frequency generating element. These components tend to be expensive and often difficult to find at the desired frequency, as they tend to cover narrow frequency ranges.

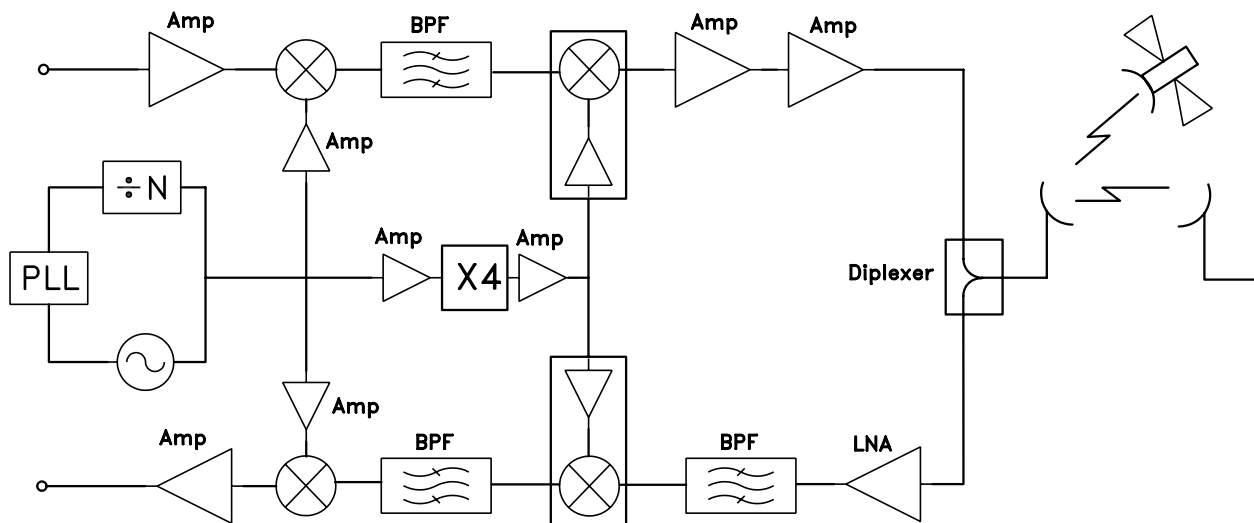


Figure 1 – Microwave radio link block diagram

Application Problem

With wireless standards going higher in frequency to take advantage of available spectrum, the required LO frequencies are also rising. With this increasing frequency comes the problem of realizing the LO generation circuitry in a simple and cost effective manner. In figure 2(a), the LO is generated with a high frequency VCO and PLL with associated filtering. This requires a high quality, high frequency oscillator and frequency divider. An alternative and common approach is to utilize a relatively low frequency oscillator cascaded with frequency multipliers to reach the required LO frequency. This alternative scheme is depicted in figure 2(b) and allows the designer to use inexpensive and widely available VCO's from the Cellular band for high frequency applications.

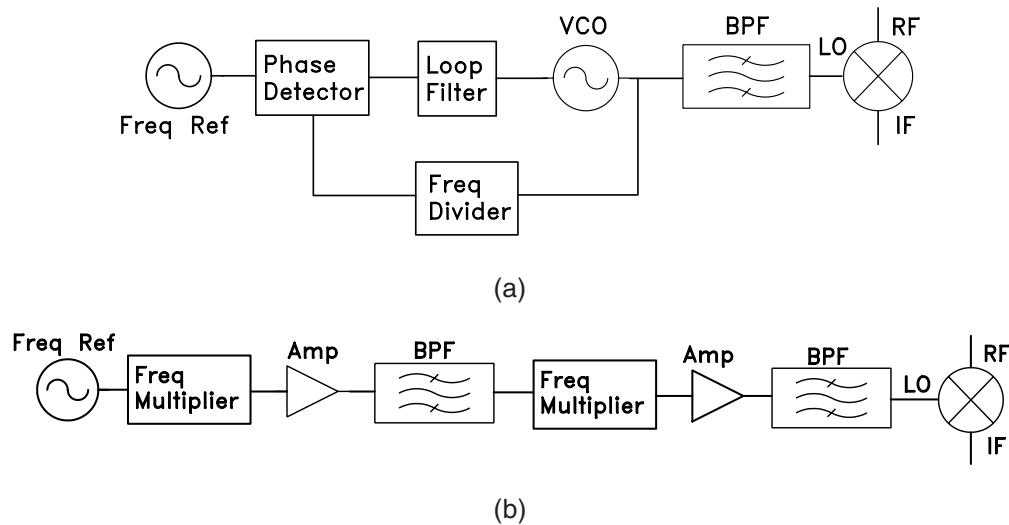


Figure 2 – LO generation via (a) PLL (b) frequency multiplication

The only remaining problem then is to realize and implement the frequency multipliers in a small and cost effective manner. Figure 3 shows a discrete diode frequency multiplier implementation, consisting of a four diode bridge and two balun transformers. This implementation has many advantages including excellent suppression of harmonics and very low residual phase noise. This circuit is realized with discrete diode bridges and baluns. While diode bridges are available in integrated packages, balun transformers are often realized with quarter-wavelength transmission lines, which are physically large at lower frequencies.

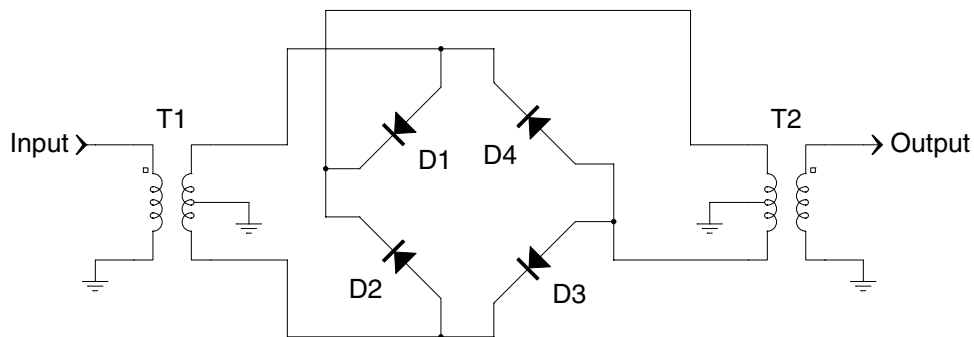


Figure 3 – Discrete implementation of a doubly balanced diode frequency multiplier

The variation of the diodes device characteristics over temperature and bias conditions tend to degrade the frequency multiplier performance making it essential that the diodes be well matched to each other. Compensating these diode bridge imperfections can be accomplished via external tuning components. However, hand tuning of these circuits in high volume production is cost prohibitive. As a result, implementing the frequency multiplier discretely will result in a relatively large and costly circuit.

Application Solution

The solution to the discrete frequency multiplier problems is a fully integrated monolithic frequency multiplier, such as the HMC189MS8. The HMC189MS8 integrates the input and output baluns directly

on the GaAs substrate with the diodes, and the entire circuit fits in a 3 mm x 5 mm package, making for a compact footprint on the PC board. The monolithic implementation of the baluns results in excellent balance and symmetry and eliminates the need for external tuning to compensate for imbalance.

Passive monolithic frequency doublers typically require +15 dBm input power to achieve conversion loss of 12 to 15 dB. However, by using input and output matching networks, conversion loss is improved while lowering the input power, thereby lessening the number of required gain stages within the multiplication chain. This product note illustrates the matching procedure for the HMC189MS8 frequency multiplier resulting in improved performance and extended operating frequency range allowing the device to be used to realize a low cost LO multiplier chain.

LO Generator

A typical application for the HMC189MS8 frequency multiplier is to convert a low frequency, low cost cellular band VCO output up to Ku band frequencies for DBS, Point-to-Point or VSAT applications. Figure 4 shows a block diagram of the 7.2 GHz LO chain required to drive a 14.4 GHz sub harmonic mixer utilizing the HMC189MS8 frequency doubler. Beginning with a VCO in the 1.8 GHz range, a common frequency for PCS Cellular applications, the HMC189MS8 is used twice to reach the mixer LO frequency at 7.2 GHz.

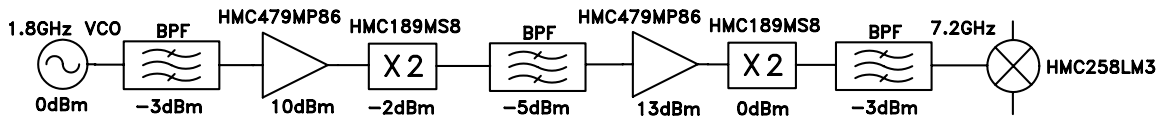


Figure 4 – Ku band LO chain

Since the first stage multiplication is at an input frequency of 1.75 GHz, we need a good input return loss at 1.75 GHz and good output return loss at 3.5 GHz. Figure 5 shows the conversion gain and input return loss of the HMC189MS8 as a function of input power measured in a 50Ω system. Inspection of figure 5(a) shows that conversion loss of the multiplier at output frequency of 3.5 GHz is approximately 17 dB with an input power of +15 dBm. Input return loss at 1.8 GHz in figure 5(b) is 5 dB, indicating that input matching is required at this frequency.

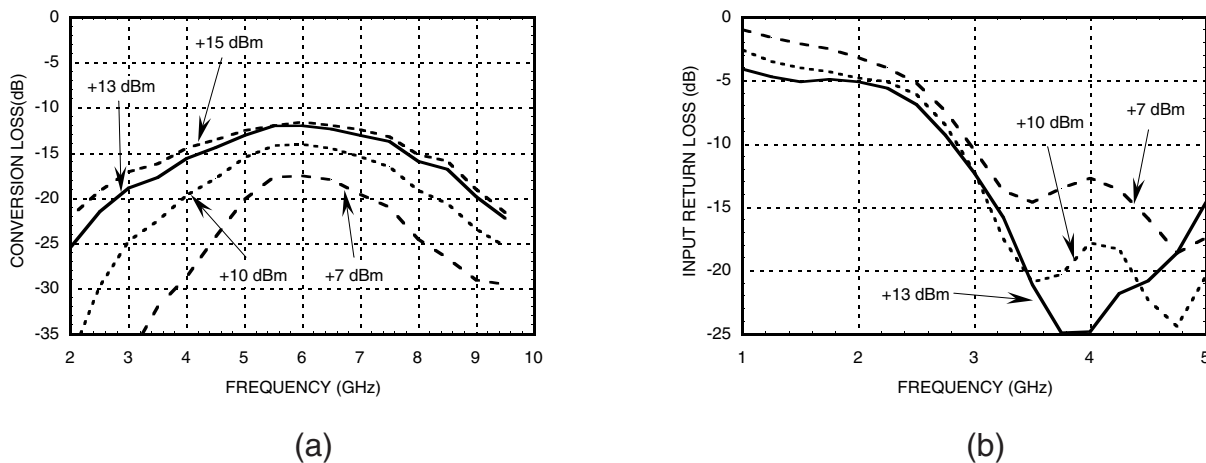


Figure 5 – (a) Conversion gain and (b) return loss versus input power

Matching Circuit Design

The first step in designing the input and output matching circuit was to measure the s-parameters of the HMC189MS8 at the desired input drive level using the test setup shown in Figure 6. This setup allowed us to simultaneously measure the conversion gain and input/output return loss. The configurable test set allowed us to boost the input signal level to the frequency doubler. Sliding loads were used at both the input and output ports to enable simultaneous matching since there is finite isolation between the output and the input.

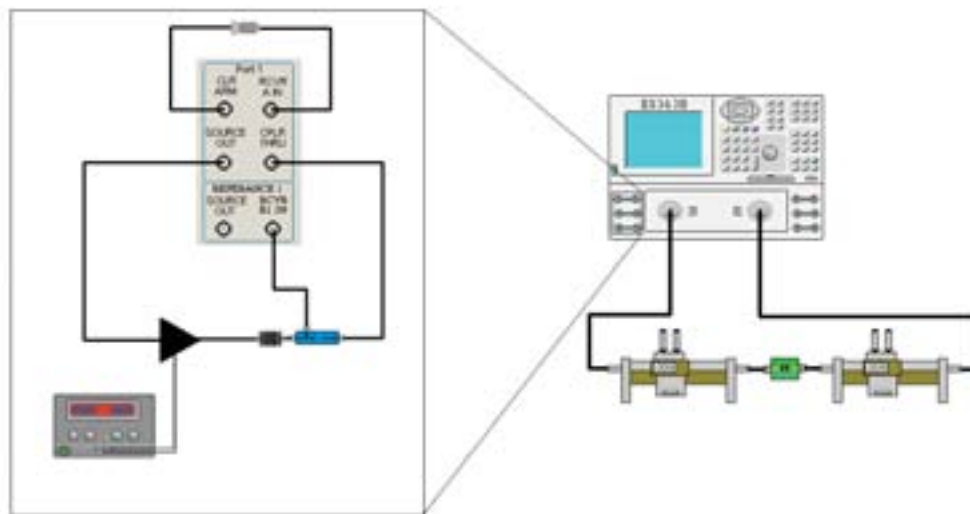


Figure 6 – S-parameter measurement test setup

This interaction between the input and output of the frequency multiplier will change the impedance seen at the other port from the value measured in 50Ω. For this reason, static 1-port s-parameter data is not useful in determining the appropriate matching conditions. This is shown in figure 7 by considering a general two-port network with arbitrary source and load impedance.

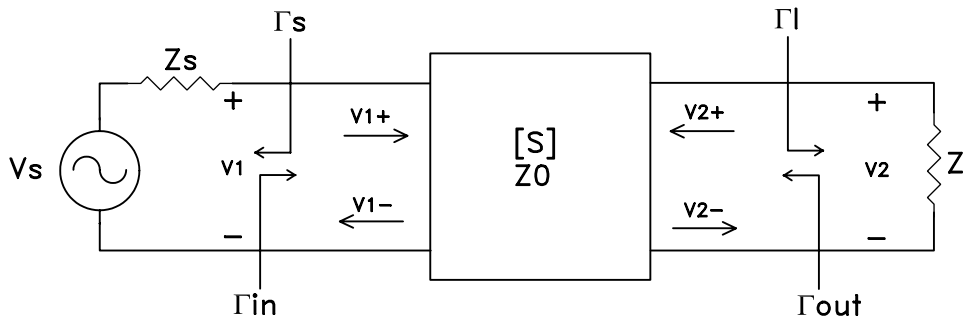


Figure 7 – Two-port network with arbitrary source and load impedances

The input reflection coefficient for an arbitrary load impedance is given by¹

$$\Gamma_{in} = \frac{V_1^-}{V_1^+} = S_{11} + \frac{S_{12}S_{21}\Gamma_l}{1 - S_{22}\Gamma_l}$$

The output reflection coefficient is correspondingly given by

$$\Gamma_{out} = \frac{V_2^-}{V_2^+} = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s}$$

Thus, for a given S_{12} and S_{21} , the actual S_{11} and S_{22} at the network ports will depend upon the source and load impedances and will not, in general, match the device s-parameters measured in 50Ω .

The tuning procedure then consisted of adjusting the input and output tuners to obtain optimum conversion gain and return loss. Beginning with the output, the sliding loads were adjusted to maximize conversion gain with an input power of +10 dBm. This was an iterative process due to interaction between input and output. Measurements of conversion loss and return loss with and without the tuners are shown in figure 8.

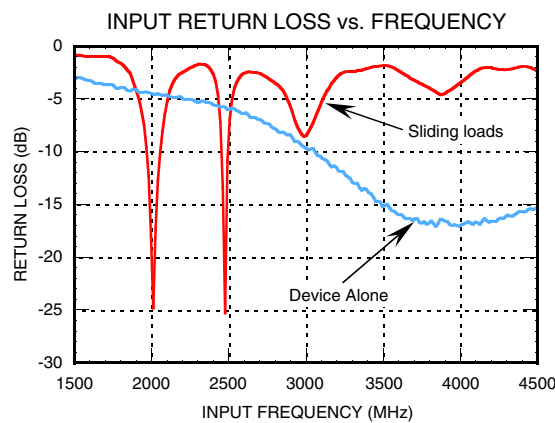


Figure 8a – Sliding load measurements of input return loss

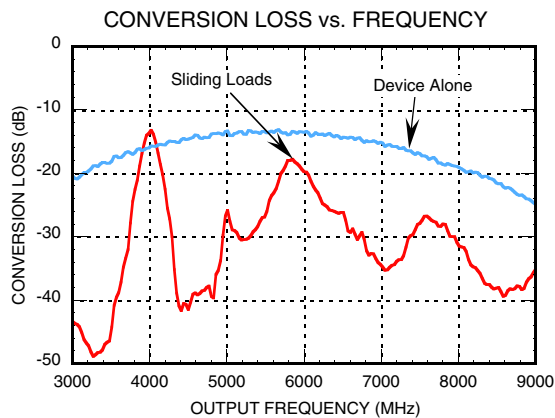


Figure 8b – Sliding load measurements of conversion loss

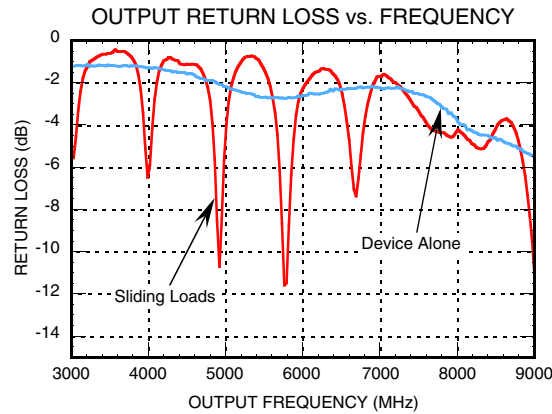


Figure 8c – Sliding load measurements of output return loss

Once the optimum performance was obtained, the sliding loads were disconnected and measured separately on the network analyzer to determine their respective impedances. The complex load impedances for both tuners are summarized in table 1.

Input Frequency (GHz)	Input Load Impedance (Ω)	Output Load Impedance (Ω)
1.7	80.7 + j 116.9	76.1 + j 221.3
2	36.0 + j 141.9	46.6 + j 186.2
2.5	29.9 + j 61.4	19.3 – j 58.9
3	26.7 – j 70.3	103.0 – j 98.2
3.5	57.0 – j 75.2	132.7 + j 105.7
4	72.8 + j 68.1	77.1 + j 128.2

Table 1 – Measured optimized load impedance for different input frequencies

Once the measured S parameter data was collected, it was necessary to de-embed the effect of the connectors and circuit board traces in order to calculate the load impedances needed at the pins of the device. This was done using Eagleware’s Genesys simulation software², by including a connector model and a short section of coplanar transmission line with dimensions matching those of the evaluation board. Figure 9(a) shows the circuit schematic used for de-embedding the load impedance data where the two-port block represents the measured load impedance of the tuner and the negation block is used to remove the effects of the evaluation board and connectors. Figure 9(b) is the measured tuner load data by itself. Figure 10 shows the result of the de-embedding graphically on a Smith chart.

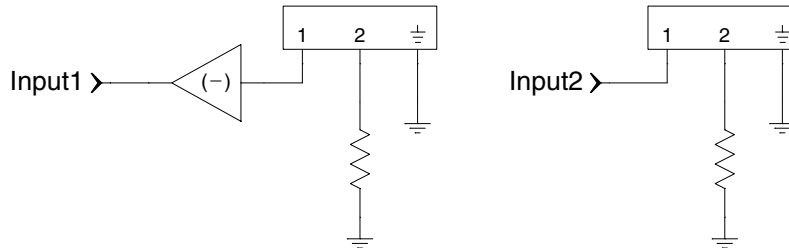


Figure 9 – (a) De-embedding circuit schematic and (b) load impedance

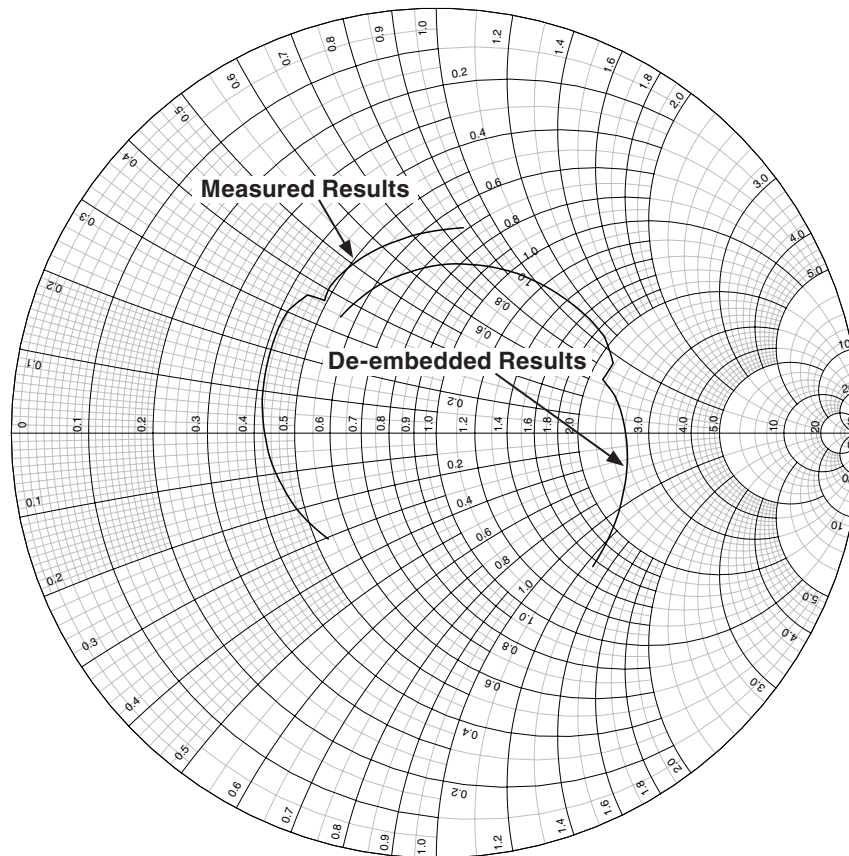


Figure 10 – Tuner load impedance

The de-embedded load impedance values were then used to synthesize the matching networks. Since the intended application is narrow band, the designs were simple two-element LC networks. Figure 11 shows one of the networks used for input matching. The designs were created by rotating a 50Ω load to present the optimal impedance to the input/output pin of the HMC189MS8 using the component tuning capability in Genesys, which allowed for real-time adjustments on the Smith chart. Figure 12 shows the results for one of the input matching networks with the two curves intersecting at the frequency of interest.

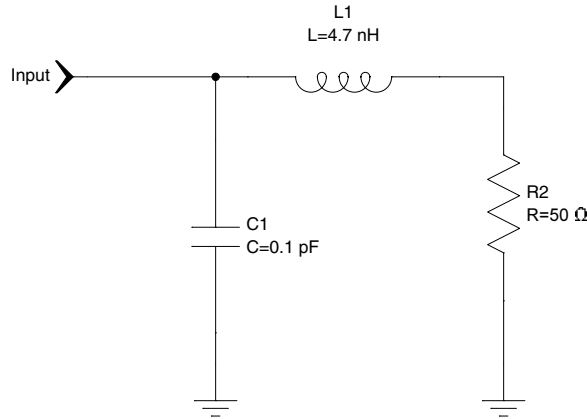


Figure 11 – Input matching network

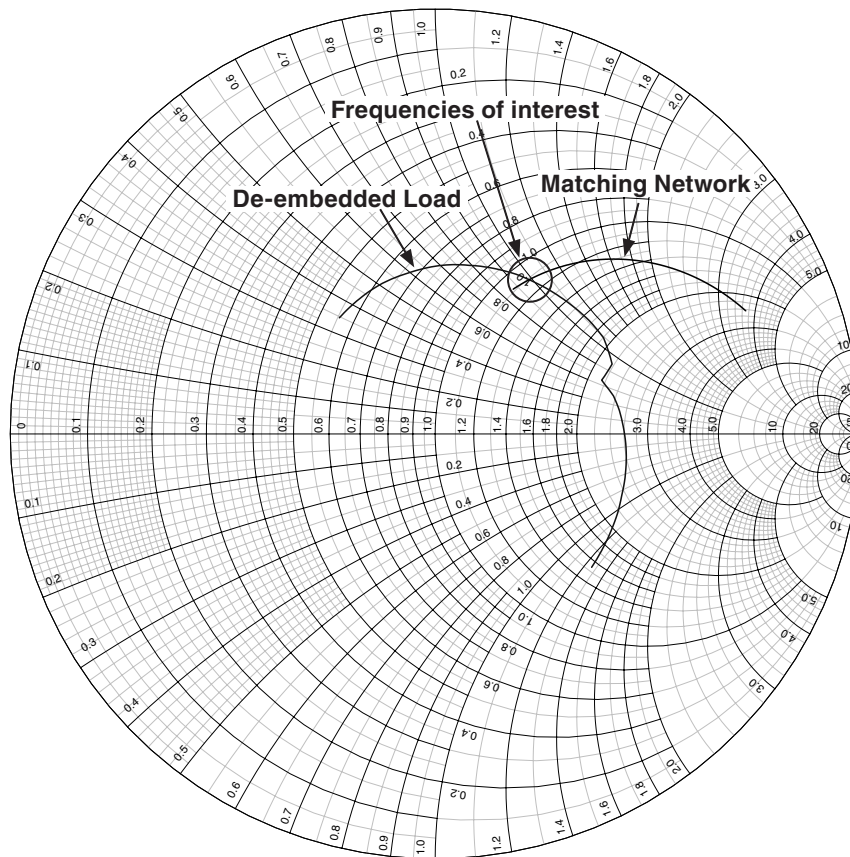


Figure 12 – Matching network load presented to the device

Matching circuit component values from the simulation are listed in table 2. These matching networks were then realized on the evaluation board for the HMC189MS8 as shown in figure 13. Some minor adjustments were made to the matching circuits in the lab that compensate for component parasitics and substrate effects. These effects were relatively minor and the resulting tuning values shown in table 3 are very close to the simulated values.

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Frequency (GHz)	Input Series Component	Input Shunt Component	Output Series Component	Output Shunt Component
1.7	4.7 nH	0.1 pF	3.9 nH	1 pF
2	3 pF	2.9 nH	2.6 nH	0.8 pF

Table 2 – Simulated matching network component values

Frequency (GHz)	Input Series Component	Input Shunt Component	Output Series Component	Output Shunt Component
1.7	4.7 nH	0.1 pF	3.9 nH	0.5 pF
2	3 pF	2.7 nH	2.7 nH	0.1 pF

Table 3 – Matching network component values from tuning

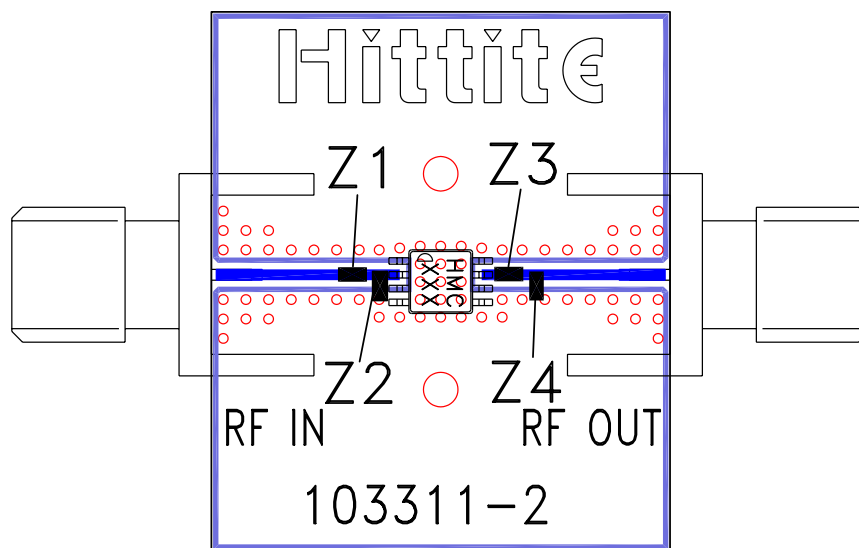
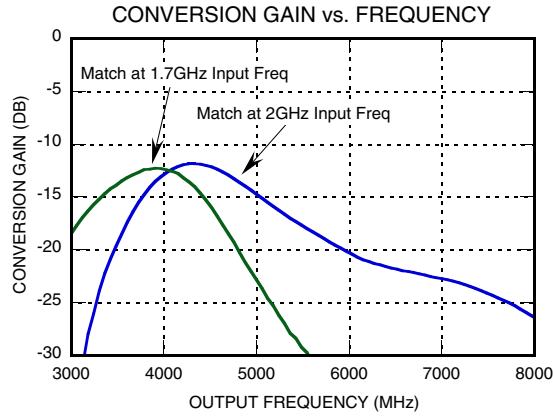


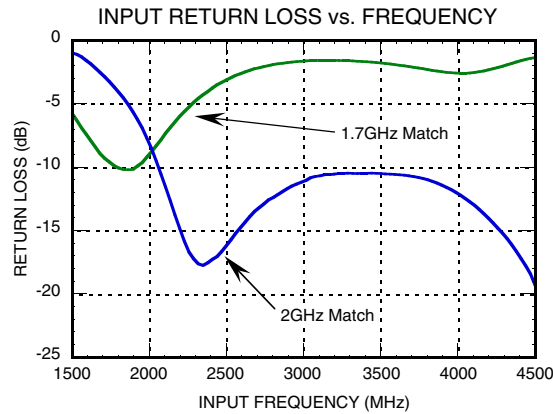
Figure 13 – Evaluation board with matching components

Measured Results

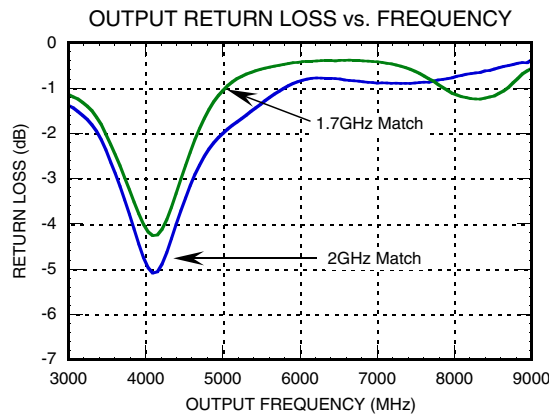
The measured conversion gain and return loss for the matched HMC189MS8 is shown in figure 14. Comparison of figure 14(a) to figure 5(a) shows approximately 10-dB improvement in conversion gain at an output frequency of 3.5 GHz and an input drive level of +10 dBm. This significant improvement allows one gain stage to be eliminated from the LO generation chain. In addition, the input and output return loss has been improved as shown in figure 14(b) and 14(c) respectively. The improved return loss will help to minimize amplitude ripple in the frequency domain.



(a)



(b)



(c)

Figure 14 – Measured Results for matched frequency multiplier
(a) conversion loss (b) input return loss (c) output return loss

Limitations

One limitation imposed by this tuning method is the resulting narrow band performance due to the simple matching topology. Alternatively, a wider-bandwidth lumped element, or distributed tuning network can be used. Broadband matching networks are inherently more complex and realizing these networks requires additional board space.

Performance improvements gained through this approach are mainly limited to the lower frequency end of the operating band where the input and output return loss of the unmatched device is relatively poor. Improvements in mid-band conversion loss were shown to be limited to approximately 1 dB by input and output tuning as expected since the device return loss was already well matched in this area.

Conclusion

By using simple two-element matching networks at the input and output of a HMC189MS8 frequency multiplier, marked improvement in conversion gain as well input and output return loss were realized, extending the operational bandwidth of the device. This was accomplished using load pull techniques simultaneously at the input and output. With a minimum of components and a standard evaluation board, a low cost frequency multiplier suitable for use in DBS, VSAT and Pt-Pt radio LO generation chain was demonstrated. This approach can be extended with modification to Hittite's entire line of passive doublers that include the HMC156, HMC158, HMC204, HMC205, HMC331, HMC156C8, HMC158C8, HMC204C8, HMC187MS8, HMC188MS8 and HMC204MS8G.

(Endnotes)

¹ David M. Pozar, "Microwave Engineering", Addison-Wesley, 1993

² Genesys, RF and Microwave Linear simulation software, Eagleware Corporation, Norcross, GA