

A voltage variable attenuator is preferable over a digital attenuator in this application since it has continuously variable attenuation. In order to maintain a flat gain response over a wide bandwidth it is important to maintain a good 50 Ω match between the VVA and IF amplifier. Many VVA's suffer from poor VSWR as their attenuation is varied since the resistive values of the attenuator may no longer present the optimum input impedance. In order to address this problem, the HMC346MS8G has incorporated an integrated reference circuit, which in conjunction with an off-chip OpAmp circuit, automatically adjusts the attenuator for optimum impedance while maintaining its' attenuation value. This product note will address the operation of this circuitry and its limitations.

HMC346MS8G VVA Circuit Description

The HMC346MS8G is comprised of three major sections (as shown in Figure 2), two of which are on-chip and the third off-chip. The two on-chip sections are the RF attenuator (Section I) and reference attenuator (Section II). Naturally, the RF attenuator is used to apply loss to the RF signal where the reference attenuator is used in conjunction with the off-chip control circuitry (Section III) to establish an optimum impedance point. In addition, the off-chip control circuitry provides a single control line interface for the VVA. Each section will be described individually beginning with the RF attenuator.

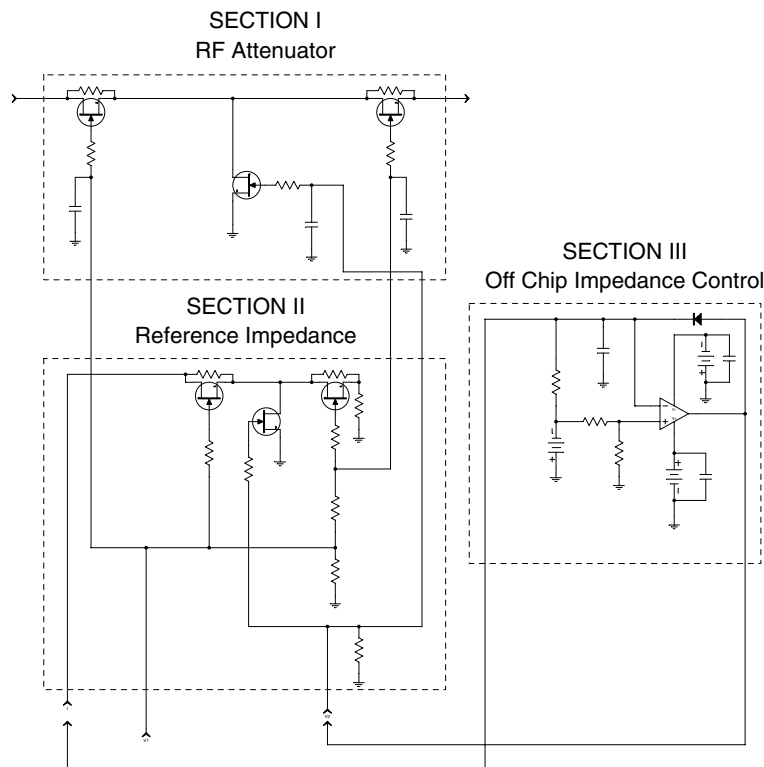


Figure 2 - HMC346MS8G Variable Voltage Attenuator with off-chip impedance control

Section 1 - RF Attenuator

The RF attenuator is based on a traditional resistive “T” topology where the FET’s are used as series and shunt resistors. The schematic shown in Figure 2 is simplified and does not include all of the circuit details. 50Ω resistors are placed in parallel with the series FET’s to improve match at the higher attenuation states. This resistance is required since during the high attenuation states the series FET’s are essentially open (or capacitive) while the shunt FET’s are essentially shorts (or small resistance) to ground.

Section II - Internal Reference Circuit

The attenuator circuit as depicted in Figure 2 requires two control lines to maintain a 50 Ω impedance match at the input and the output over the full attenuation range. Maintaining this 50 Ω match requires a specific complementary relationship between V1 and V2. The on-chip reference circuit is used with the off-chip OpAmp circuit to determine and set the V2 voltage in order to maintain a 50 Ω match. This reference attenuator is depicted in “Section II” of Figure 2 and below in Figure 3.

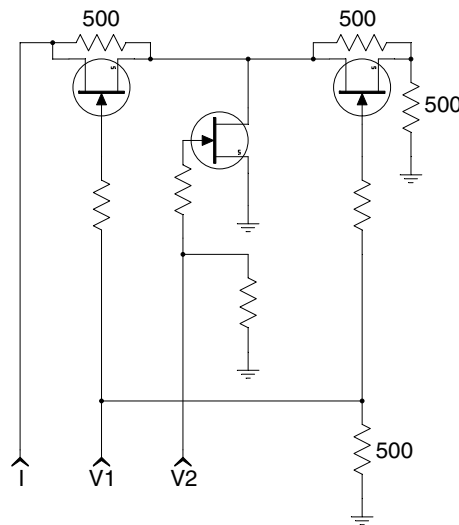


Figure 3 - Schematic of the on-chip reference attenuator circuit

The reference attenuator has the same “T” topology as the RF attenuator with the exception that the resistors parallel to the series FET’s are 500 Ω instead of 50 Ω and the characteristic impedance of the reference attenuator is 500Ω . This 10:1 ratio will allow for the external impedance circuit to simultaneously adjust the impedance of both the RF and reference attenuators. For example, if 0V is applied to the series FET in the RF attenuator the channel resistance will be 7.7 Ω , which corresponds to 77 Ω with the same voltage applied to the series FET on the reference attenuator. The off-chip impedance control circuit continually adjusts the V2 voltage maintaining 500 Ω characteristic impedance at the input of the reference attenuator. Because of the 10:1 relationship, the RF attenuator will be maintained at 50 Ω.

Section III - Off-chip Impedance Control Circuit

The reference attenuator used with the external OpAmp circuit provides a single-line voltage control as well as the return loss tracking for the RF attenuator circuit. The external OpAmp circuit depicted in Figure 4 forms a control loop with the reference attenuator and adjusts control voltage V2 such that the impedance seen looking into port I is always adjusted to 500 Ω for any given V1 value. The input to the non-inverting terminal (V_{REF}) consists of a voltage divider that is made up of a 500 Ω resistor to ground and a 3.9k Ω resistor to a -5V reference voltage. The inverting input sees a voltage (V_I) divider consisting of a 3.9k Ω resistor to the same -5V reference voltage and the reference attenuator. The output of the OpAmp is equal to:

$$V2 = -A \cdot (V_I - V_{REF}) \quad (1)$$

where:

- A = Open Loop Gain (V/V)
- V_I = Voltage at the I port (V)
- V_{REF} = Non-inverting input voltage (V)

The OpAmp control loop forces V_1 to track V_{REF} by forcing V_2 to a voltage that sets the reference attenuator impedance looking into port I to 500Ω .

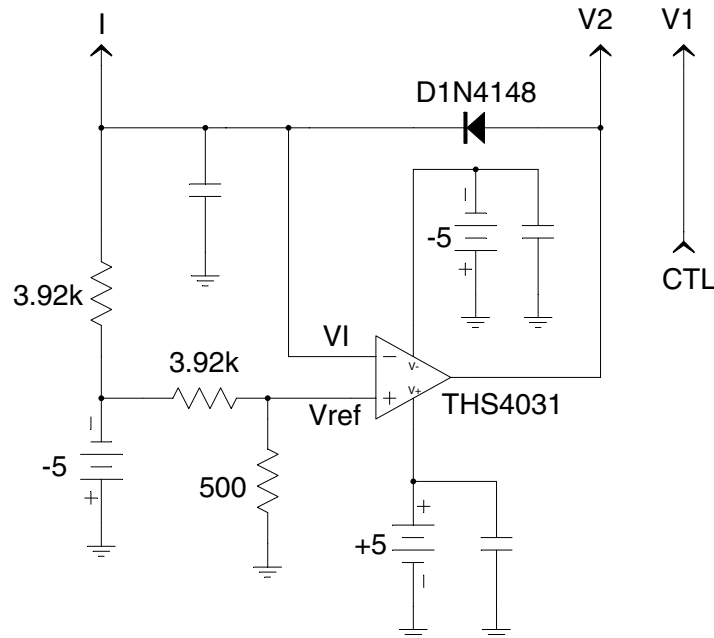


Figure 4 - Schematic of the external OpAmp circuit

Normal operation of the VVA requires that the gates of the FET's are not positively biased. For this reason a diode is placed at the output feeding back to the inverting input of the OpAmp. If the output voltage of the OpAmp attempts to swing positive, the diode will turn on and feed a positive voltage back into the inverting input. From equation (1) it can be seen that with a positive voltage in the inverting input the subsequent output will become negative.

Due to the presence of the diode, the resistor values chosen in the divider network are crucial. Since the reference attenuator impedance is 500Ω the resistance R_3 from the non-inverting input to ground must also be 500Ω . The resistors R_1 and R_2 in the voltage divider should be chosen to allow the output V_2 to get as close to zero as possible. With a $3.9K \Omega$ resistor, the voltages at the inputs of the OpAmp are about $-0.56V$. This allows the output to reach $0V$ prior to the diode turning on. If the resistors were set lower, to $1k \Omega$ for example, the voltage at the input of the OpAmp and the anode of the diode would be about $-1.7V$ causing the diode to turn on when the output of the OpAmp was around $-0.9V$. Since the diode would prevent the output from going below $-0.9V$ the full range of the attenuator could not be achieved.

The reference attenuator (Section II) and OpAmp circuit (Section III) combination were simulated using =HARBEC=. The OpAmp is simulated using a spice model provided by Texas Instruments for the THS4031 OpAmp. The diode model used is a spice model for the D1N4148 switching diode, which is provided by Fairchild Semiconductor. The reference attenuator FET's are modeled using parameters, which are provided by the vendor.

In Figure 5, the horizontal axis is the control voltage V_1 that is applied to the attenuator series FET's. The vertical axis is the output from the OpAmp that is fed back into input V_2 of the attenuator. V_2 is applied directly to the shunt FET's in both the RF and reference attenuators. The simulation clearly shows that when resistors R_1 and R_2 are $1k \Omega$ the maximum output from the OpAmp is limited to approximately $-1.0V$. This voltage would not be positive enough to achieve maximum attenuation from the attenuator. Conversely, when $3.9k \Omega$ resistance is used the maximum output voltage of the OpAmp is approximately $0V$. This is adequate to achieve the full attenuation range of the attenuator.

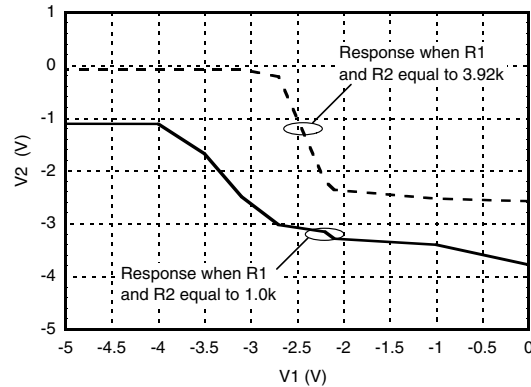


Figure 5 - Output OpAmp voltage V2 versus control voltage V1

Model of OpAmp and Reference Attenuator Control Loop

The circuits in Figure 3 and Figure 4 are combined to form a single model, which will simulate the interaction of the operational amplifier circuit with the reference circuit located within the HMC346MS8G. Figure 6 shows the results of the =HARBEC= DC analysis, which is a plot of control voltage V1, and the output V2 versus the attenuation in dB. The measured results from the Hittite evaluation board are plotted for comparison.

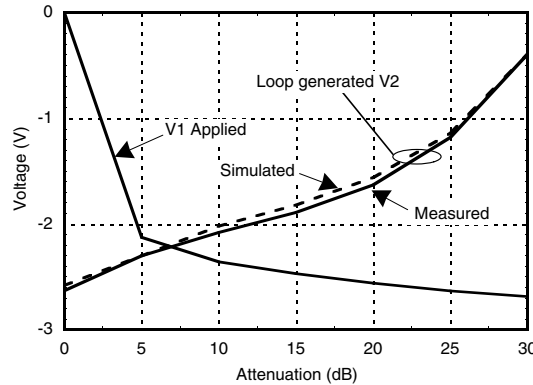


Figure 6 - V1 and V2 versus attenuation

Inspection of Figure 6 reveals how the VVA operates with varying control voltage. At 0dB attenuation V1 is at its maximum and V2 is at its minimum, at which point the series FET’s are on and the shunt FET is off. The combined series resistance of the two series FET’s is 14 Ω, which results in a return loss of 18dB and insertion loss just over 1dB. At 30dB attenuation, V2 is maximum, which turns on the shunt FET. However, V1’s voltage is at its minimum value, turning the series FET’s off. Since the series FET’s present high impedance, the predominant impedance is the parallel 50 Ω resistor, which is in series with the shunt FET to ground resulting in an optimal return loss.

It is important to note that the control circuit adjusts the RF attenuator impedance to 50 Ω at DC. Therefore, the match at higher frequencies will ultimately degrade due to reactive parasitics.

Description of the Application Evaluation Board

The application evaluation board used in the measurements is shown in Figure 7. The board is constructed of Rogers RO4350, with a thickness of 10 mils. To provide rigidity to the board additional layers of Rogers RO4403 and Rogers RO4350 are used resulting in a total board thickness of 62 mils. The operational amplifier

used is the Texas Instruments THS4031. This OpAmp was selected for its speed and low noise performance. However, an alternative amplifier could be the lower cost TL343 also from Texas Instruments. For the most part, any operational amplifier can be used as long as the output is capable of the entire tuning voltage range of the attenuator and the noise and slew rate is sufficient for the application.

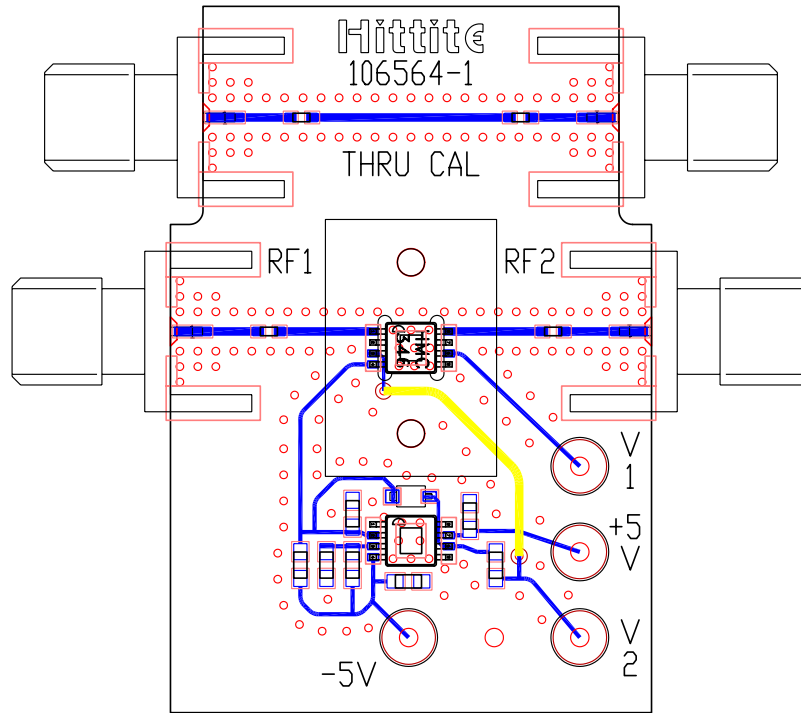


Figure 7 - HMC346MS8G evaluation board

Important Considerations When Using the HMC346MS8G

Control Line Ripple and Noise

Since a voltage applied to the control line varies the amplitude of the RF signal, a VVA acts as an amplitude modulator. Therefore, any ripple on the control line will result in AM sidebands on the RF output. An amplitude-modulated signal consists of a carrier signal and two side band signals located above and below the carrier frequency. Multiple sidebands can appear at the output depending on the number and amplitude of unwanted signal(s) appearing on the control line of the VVA. An amplitude modulated signal $m(t)$, can be written as:

$$m(t) = k_a \cdot A_m \cdot \text{Cos}(2\pi f_m t) \quad (2)$$

where K_a is a constant and A_m is the amplitude of the modulating signal. If the above signal is applied to the control line V1 of the attenuator then the output signal can be represented by:

$$S(t) = A_c \cdot [1 + m(t)] \cdot \text{Cos}(2\pi f_c) \quad (3)$$

After substituting equation (2) into equation (3) and applying the appropriate trigonometric identities, equation (3) can be expressed as:

$$S(f) = A_c \cdot \text{Cos}(2\pi f_c) + \frac{1}{2} \cdot \mu \cdot A_c \cdot \text{Cos}[2\pi(f_c - f_m)t] + \frac{1}{2} \cdot \mu \cdot A_c \cdot \text{Cos}[2\pi(f_c + f_m)t] \quad (4)$$

where $\mu = K_a \cdot A_m$. Figure 8 shows a plot of attenuation vs. control voltage V1. As depicted in the plot, $K_a = \frac{dA}{dV1} \left(\frac{1}{V}\right)$ which is the amplitude sensitivity to the control voltage V1.

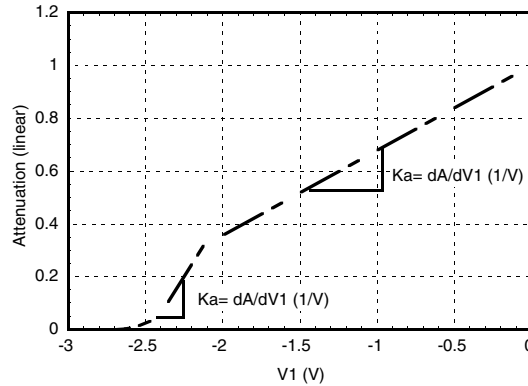


Figure 8 - Attenuation versus control voltage

The slope of the line varies from 0V to -2.5V with the slope reaching a maximum between V1=-2.25V and V1=-2.5V. From equation (4) the voltage amplitude of the sideband is equal to $V = \frac{1}{2} \cdot \mu \cdot A_c$ which is a function of the amplitude sensitivity K_a , implying that the sideband will be at a maxima when K_a is maximum.

The average power delivered to a 50Ω load is determined by:

$$P_w = \frac{V^2}{2 \cdot 50} \quad (W) \quad (5)$$

Substituting the side band voltage V into equation (5) results in the following equation:

$$P_{SideBand} = 30 + 10 \cdot \text{Log}(0.0025 \cdot \mu^2 \cdot A_c^2) \quad (\text{dBm}) \quad (6)$$

where:

$$\mu = \frac{dA}{dV1} \cdot A_m \quad (V/V)$$

A_c = The amplitude (peak) of the input signal (V)

A_m = The amplitude (peak) of the modulating signal (V)

Equation (6) can be used to calculate the power level of the sideband for given amplitude of ripple applied to the V1 control line on HMC346MS8G attenuator.

EXAMPLE:

Using evaluation board shown in Figure 7, a modulating signal with amplitude of 5 mV_{p-p} at a frequency of 100 kHz is applied to the control voltage input V1. The DC voltage on V1 is set to the following values: V1=0, -2.125, -2.357, -2.470, -2.559, -2.633, -2.687 and an RF signal of 1 GHz and amplitude of 0.1 V_{p-p} is applied to the input of the attenuator. The side band power is measured and compared to the calculated values for each value of V1.

In order to calculate the values for K_a an equation is curve fitted to the data in Figure 8. Figure 9 shows the plotted data from $-2.125V$ to $-3V$ and the polynomial that is used to determine K_a . A similar polynomial is determined for the data from $0V$ to $-2.125V$.

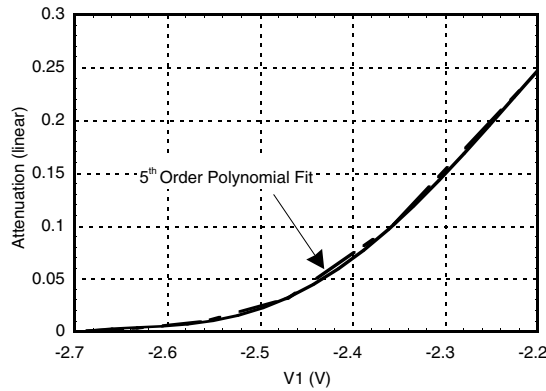


Figure 9 – Attenuation versus V1 with polynomial curve fit

The derivative of the polynomial fit function in Figure 9 is taken and multiplied by the peak voltage of the modulating signal ($0.0025V$) resulting in an equation for the modulation index μ which is a function of V1. The calculated values of the modulation index (μ) and the amplitude of the input carrier A_c are substituted into equation (6) and the sideband power calculated.

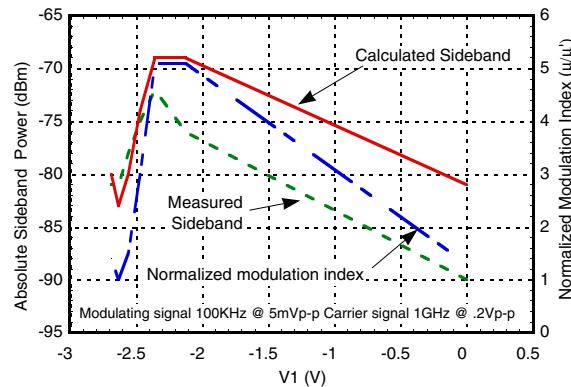


Figure 10 - Sideband power and normalized modulation index versus control voltage V1

Figure 10 is a comparison between the measured and calculated power of the sideband, which is produced when a $100kHz$ signal with an amplitude $5mV_{p-p}$ is applied to the V1 control line. Also plotted in Figure 10 is the normalized modulation index μ/μ' , which is the modulation index normalized to the minimum value (μ'). From the figure it can be seen that the maximum sideband level occurs at a control voltage V1 of approximately $-2.3V$, where the modulation index is at its maximum.

The equation gives a conservative estimate of the sideband levels with closer agreement occurring at the worst-case sideband levels. The difference between the calculated and measured is primarily due to the omission of the effects of the control loop in the calculation. Including the effects of the control loop is beyond the scope of this product note and therefore was omitted.

Switching Speed

The HMC346MS8G has a fast turn on time of 8 nSec and a rise/fall time of 2 nSec. However, when controlled by the off-chip impedance control circuit, these times will increase due to the slew rate of the operational amplifier, and circuit time constants.

For example, the THS4031 operational amplifier from Texas Instruments has a slew rate of 80 V/ μ S when operating at 5V. From previous analysis it was shown that the output of the amplifier is required to swing from -2.7V to -0.39V when switching from 0dB of attenuation to 30dB attenuation. In order to achieve this swing the operational amplifier will require 36nS, which will add to the total switching time of the attenuator. Therefore, for applications requiring fast switching the selection of a high-speed operational amplifier along with careful board design is critical.

Conclusion

The HMC346MS8G, with its on-chip reference attenuator, is a versatile voltage variable attenuator that may be implemented in a variety of gain control applications. This product note has covered, in detail, the design and theory of operation of the HMC346MS8G VVA attenuator in conjunction with an off-chip control circuit.

Depending on the application, the attenuator may be used with or without the off-chip impedance control circuit. When using the off-chip impedance control circuit special care must be taken in choosing the proper component values to ensure proper operation over the entire dynamic range. Also, because the HMC346MS8G is essentially an AM modulator, filtering of the control line may be required to minimize AM noise and spurs at the output of the attenuator.

(Endnotes)

¹ =HARBEC=, Harmonic Balance Simulator, Eagleware Corporation, Norcross, Georgia 30071

HMC346MS8G PRODUCT NOTE

Notes: