
Lock Detect Control of PLLs with Integrated VCO Products

Purpose

This application note is intended to serve as a supplement to Hittite Microwave’s Product Operating Guide entitled PLLs with Integrated VCO - RF Applications. You will find a full product listing and a link to download the datasheet for each of Hittite’s PLLs w/Integrated VCO products at www.hittite.com.

This application note captures the relevant detailed analysis regarding customer questions concerning lock detect window functionality and optimal lock detect window selection when operating in the digital window lock detect mode. Analog window functionality is also discussed. Lock detect window size selections were verified with laboratory measurements at room temperature. Variations of lock detect window size due to temperature are also considered.

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1.0 General Parameters Associated with Lock Detect

For lock detection to properly occur the Average Phase Offset must be set to allow the lock conditions shown in Figure 1 to occur within the lock window.

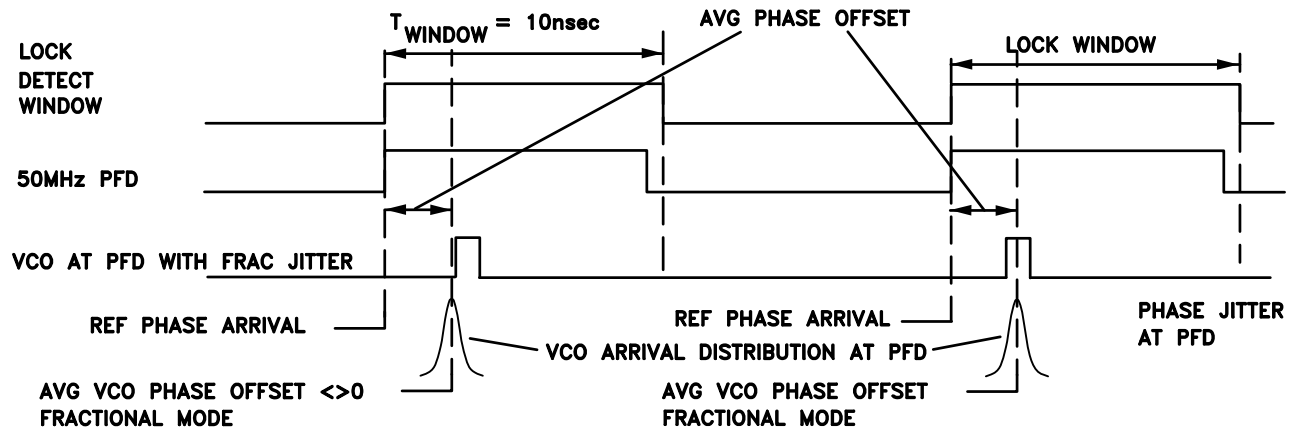


Figure 1. Lock Detect Window Timing Diagram for Fractional Mode with Offset

The Average Phase Offset is dependant on variables such as the Phase Detector (PD) period, the Charge Pump Offset Current, and the Charge Pump Gain Current. Often the Charge Pump Offset Current has to be increased to a larger value in order to improve phase-lock loop (PLL) spurious performance. This may increase the Average Phase Offset to a value that does not allow lock conditions to occur within the lock window, and then a more suitable value of ring oscillator configuration and one shot duration may have to be set in order to select an optimal lock detect window value from the allowable settings shown in Table below.

Table 1. Digital Lock Detect Window Allowable Settings Shown in Red

LD Timer Speed Reg07[11:10]	Digital Lock Detect Window Nominal Value $\pm 25\%$ (ns)							
Fastest 00	6.5	8	11	17	29	53	100	195
01	7	8.9	12.8	21	36	68	130	255
10	1.7	9.2	13.3	22	38	72	138	272
Slowest 11	7.6	10.2	15.4	26	47	88	172	338
LD Timer Divide Setting Reg07[9:7]	0	1	2	3	4	5	6	7
LD Timer Divide Value	0.5	1	2	4	8	16	32	64

The following variable parameters will be used in examples of charge pump offset current calculation and optimal lock detect window size selection:

- T_{VCO} = VCO period at the PLL feedback into the prescaler
- F_{comp} = The comparison frequency in the Phase Detector (PD)
- PD_{period} = The Phase Detector period
- CP_O = Charge Pump offset current
- I_{CP} = Charge Pump gain current
- $Offset_{avg}$ = Average Phase Offset

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- $\text{Offset}_{\text{nominal}}$ = Nominal Phase Offset
- $\text{Geometric}_{\text{mean}}$ = Geometric mean calculation of optimal lock detect window
- $\text{LD}_{\text{window}}$ = Lock Detect Window size

2.0 Charge Pump Offset Current Example Calculation

The charge pump offset current is directly dependant on the VCO period at the PLL feedback into the prescalar, the comparison frequency, and the charge pump gain current.

$$T_{\text{VCO}} = \frac{1}{2 \text{ GHz}} = 0.5 \text{ ns} \quad F_{\text{comp}} = 25 \text{ MHz} \quad I_{\text{CP}} = 2000 \mu\text{A}$$

$$\text{CP}_O = (2 \text{ ns} + 4 \cdot T_{\text{VCO}}) \cdot (F_{\text{comp}}) (I_{\text{CP}})$$

$$\text{Therefore: } \text{CP}_O = 200 \mu\text{A}$$

3.0 Average Phase Offset Calculation & Optimal Lock Detect Window Size Selection

The average phase offset must be set to fit within the lock window as shown in Figure 1. The average phase offset is dependant on the phase detector period, the charge pump offset current, and the charge pump gain current.

$$\text{PD}_{\text{period}} = \frac{1}{F_{\text{comp}}} = 40 \text{ ns}$$

$$\text{Offset}_{\text{avg}} = \frac{\text{CP}_O}{I_{\text{CP}}} \text{PD}_{\text{period}} = 4 \text{ ns}$$

The nominal phase offset and geometric mean calculations take into account changes that occur in temperature (+25% for 85°C or -25% for -40°C) range and are therefore used for optimal lock detect window size selection.

$$\text{Offset}_{\text{nominal}} = \text{Offset}_{\text{avg}} \cdot 1.25 = 5 \text{ ns}$$

$$\text{Geometric}_{\text{mean}} = \sqrt{\text{Offset}_{\text{nominal}} \cdot \text{PD}_{\text{period}}} = 14.142 \text{ ns}$$

Using the geometric mean of 14.142 ns we now look for a suitable value of ring oscillator configuration and one shot duration as shown in the Table below.

Table 2. Digital Lock Detect Window Selection for Geometric Mean = 14.142 ns

LD Timer Speed Reg07[11:10]	Digital Lock Detect Window Nominal Value $\pm 25\%$ (ns)							
Fastest 00	6.5	8	11	17	29	53	100	195
01	7	8.9	12.8	21	36	68	130	255
10	1.7	9.2	13.3	22	38	72	138	272
Slowest 11	7.6	10.2	15.4	26	47	88	172	338
LD Timer Divide Setting Reg07[9:7]	0	1	2	3	4	5	6	7
LD Timer Divide Value	0.5	1	2	4	8	16	32	64

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If CP_O was set to 600 μ A then:

$$CP_O = 600 \mu\text{A}$$

$$\text{Offset}_{\text{avg}} = \frac{CP_O}{I_{CP}} \quad PD_{\text{period}} = 12 \text{ ns}$$

$$\text{Geometric}_{\text{mean}} = \sqrt{\text{Offset}_{\text{nominal}} \cdot PD_{\text{period}}} = 24.495 \text{ ns}$$

Table 3. Digital Lock Detect Window Selection for Geometric Mean = 24.495 ns

LD Timer Speed Reg07[11:10]	Digital Lock Detect Window Nominal Value $\pm 25\%$ (ns)							
Fastest 00	6.5	8	11	17	29	53	100	195
01	7	8.9	12.8	21	36	68	130	255
10	1.7	9.2	13.3	22	38	72	138	272
Slowest 11	7.6	10.2	15.4	26	47	88	172	338
LD Timer Divide Setting Reg07[9:7]	0	1	2	3	4	5	6	7
LD Timer Divide Value	0.5	1	2	4	8	16	32	64

This lock detect window size selection can vary $\pm 25\%$ due to temperature and therefore:

$$LD_{\text{window}} = 26 \text{ ns}$$

$$+25\% \text{ at } +85 \text{ }^\circ\text{C}: LD_{\text{window}} \cdot 1.25 \cdot 32.5 \text{ ns} < PD_{\text{period}} \cdot 40 \text{ ns}$$

$$-25\% \text{ at } -40 \text{ }^\circ\text{C}: LD_{\text{window}} \cdot 0.75 \cdot 19.5 \text{ ns} > \text{Offset}_{\text{nominal}} \cdot 15 \text{ ns}$$

This lock detect window size selection is therefore suitable for both the phase detector period and the worst case phase offset value.

4.0 Laboratory Measurements of Lock-Detect Capability

Actual measurements in the laboratory show that an even smaller lock detect window size setting of 17ns is possible for operation at room temperature as shown in Table 4. The two lock failures above 40ns are predictable as these first two settings are greater than one lock window period. By the 68ns setting lock is being detected by the second cycle in the lock window period. The failures at 138ns, 272ns, and 338ns are more difficult to predict because the variances and geometric means of multiple lock window cycles must be considered, as well as potential process variance.

Table 4. Laboratory Lock Detect Results for Various Lock Detect Window Values

LD Timer Speed Reg07[11:10]	Digital Lock Detect Window Nominal Value $\pm 25\%$ (ns)							
Fastest 00	6.5	8	11	17	29	53	100	195
01	7	8.9	12.8	21	36	68	130	255
10	1.7	9.2	13.3	22	38	72	138	272
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LD Timer Divide Value	0.5	1	2	4	8	16	32	64

■ = Failed to Lock ■ = Locked Ok

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5.0 Analog Window Lock Detect

For Analog mode the Lock Detect Register 07h Bit [6] must be set to a value of zero, and the phase offset, as calculated earlier, must have a result that can fit within the fixed analog 10ns lock window size as shown in Figure 2.

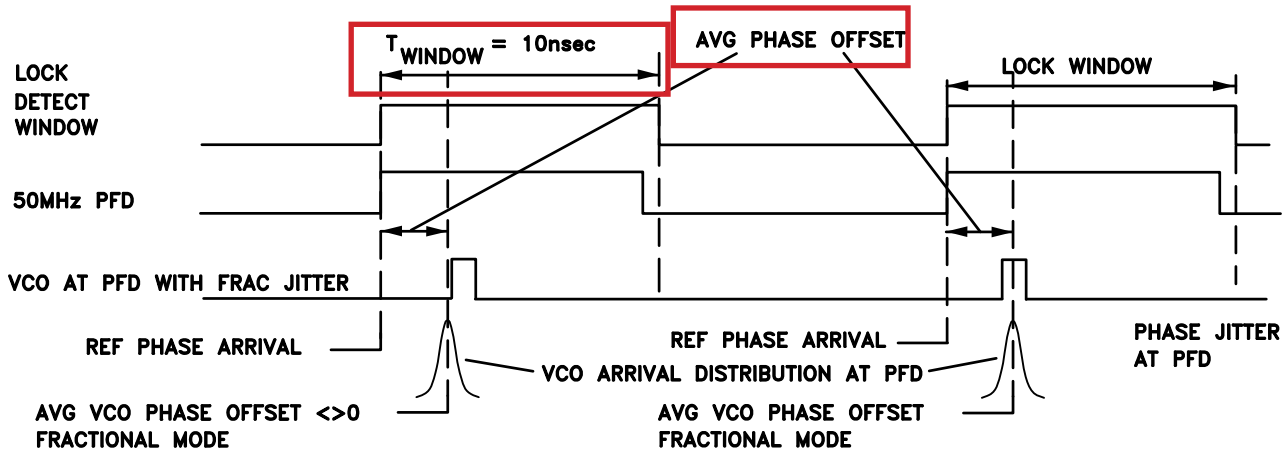


Figure 2. Timing Diagram showing Fixed Analog 10ns Lock Window

Using a Charge Pump offset current of 600 μA for optimum PLL spurious performance results in an average phase offset that will overshoot the analog lock detect window size of 10ns, and it is therefore necessary to use the digital window lock detect mode because of this design constraint.

6.0 Optimal Lock Detect Window Calculations Using a Comparison Frequency of 50 MHz

When the comparison frequency is increased while holding all the other dependant variables constant then the optimal lock detect window size will be significantly decreased.

$$F_{\text{comp}} = 50 \text{ MHz} \quad C_{\text{P}0} = 600 \mu\text{A} \quad I_{\text{CP}} = 2000 \mu\text{A} \quad \text{PD}_{\text{period}} = \frac{1}{F_{\text{comp}}} = 20 \text{ ns}$$

$$\text{Offset}_{\text{avg}} = \frac{C_{\text{P}0}}{I_{\text{CP}}} \cdot \text{PD}_{\text{period}} = 6 \text{ ns} \quad \text{Offset}_{\text{nominal}} = \text{Offset}_{\text{avg}} \cdot 1.25 = 7.5 \text{ ns}$$

$$\text{Geometric}_{\text{mean}} = \sqrt{\text{Offset}_{\text{nominal}} \cdot \text{PD}_{\text{period}}} = 12.247 \text{ ns}$$

Using the geometric mean of 12.247 ns we now look for a suitable value of ring oscillator configuration and one shot duration as shown in Table 5.

Table 5. Laboratory Lock Detect Results for Various Lock Detect Window Values

LD Timer Speed Reg07[11:10]	Digital Lock Detect Window Nominal Value $\pm 25\%$ (ns)							
Fastest 00	6.5	8	11	17	29	53	100	195
01	7	8.9	12.8	21	36	68	130	255
10	1.7	9.2	13.3	22	38	72	138	272
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This lock detect window size selection can vary $\pm 25\%$ due to temperature and therefore:

$$LD_{\text{window}} = 12.8 \text{ ns}$$

$$+25\% \text{ at } +85 \text{ }^\circ\text{C}: LD_{\text{window}} \bullet 1.25 \bullet 16 \text{ ns} < PD_{\text{period}} \bullet 20 \text{ ns}$$

$$-25\% \text{ at } -40 \text{ }^\circ\text{C}: LD_{\text{window}} \bullet 0.75 \bullet 9.6 \text{ ns} > \text{Offset}_{\text{nominal}} \bullet 7.5 \text{ ns}$$

This lock detect window size selection is therefore suitable for both the phase detector period and the worst case phase offset value.

7.0 Summary of Calculation Results

The optimal digital lock detect window size settings calculated in the all the earlier examples are summarized in Table 6. These numbers include how much the window size is expected to change with extreme changes in temperature.

Table 6. Summary of Optimal Digital Lock Detect Window Control Parameters

F_{comp}	PD_{period}	I_{CP}	CP_{O}	W	$W +25\%$	$W -25\%$
25 MHz	40 ns	2 mA	0.2 mA	15.4 ns	19.25 ns	11.55 ns
25 MHz	40 ns	2 mA	0.6 mA	26.0 ns	32.50 ns	19.50 ns
50 MHz	20 ns	2 mA	0.6 mA	12.8 ns	16.00 ns	9.60 ns

F_{comp} = Comparison Frequency

PD_{period} = Phase Detector Period = $1 / F_{\text{comp}}$

I_{CP} = Charge Pump Gain Current

CP_{O} = Charge Pump Offset Current

W = Optimal Lock Detect Window Size

$W+25\%$ = Lock Detect Window Size at $+85 \text{ }^\circ\text{C}$

$W-25\%$ = Lock Detect Window Size at $-40 \text{ }^\circ\text{C}$