Analog Devices Welcomes Hittite Microwave Corporation

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Introduction

This document presents the characteristics of the HMCAD1520 A-to-D converter in the 12 bit high-speed mode and the 14 bit precision mode.

The presented measurement results are either the uncompensated output directly from the A-to-D converter, or results that are compensated for gain mismatch, time skew and offset. The compensated results are compensated by post processing of the A-to-D output codes. The post processing use the 12 bit ADC output as input, calculates a gain compensation with 16 bit, and trunacates the result to 14 bit resolution. All the precision mode (14 bit) measurements are uncompensated.

The report presents measurements of:

• Input frequency, Fin, sweeps
• Sampling frequency, FS, sweeps
• Common mode voltage, Vcm, sweeps
• Different bias control settings
• Temperature sweeps
• Supply voltage sweeps
• Different gain settings
• Different clock jitter control settings
• Common mode output buffer voltage
• Power consumption in different settings
• Time skew measurements

Characterization Setup

The measurements were carried out utilizing the equipment listed in Table 1.

<table>
<thead>
<tr>
<th>Equipment use</th>
<th>Description</th>
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<tbody>
<tr>
<td>Mother Board</td>
<td>Xilinx Spartan-6 FPGA SP601 Evaluation Kit</td>
</tr>
<tr>
<td>Clock Source</td>
<td>HMC830</td>
</tr>
<tr>
<td>Signal Source</td>
<td>Hewlett Packard 8644B</td>
</tr>
<tr>
<td>Band Pass Filters</td>
<td>TTE KC4T- and Q56T-series</td>
</tr>
<tr>
<td>EVAL01-HMCAD1520</td>
<td>Evaluation card for the HMCAD1520 A-to-D converter</td>
</tr>
</tbody>
</table>

See Figure 1 for Measurement setup.
Figure 1: Measurement setup
Analog Input Network
All measurements, unless otherwise noted, are done with a balun input. The input network of the test setup is as described in Figure 2.

![Analog input network with transformer](image)

**Figure 2: Analog input network with transformer**

Clock Source and Input
The clock network is a balun coupling. It is as described in Figure 3. The diodes are for input protection at large signal swings.

![Clock input network](image)

**Figure 3: Clock input network**
Compensation
The output of the HMCAD1520 is gain mismatch, time skew and offset compensated by post processing of the ADC output. The post processing use the 12 bit ADC output as input, calculates the gain mismatch, time skew and offset with 16 bit, and truncates the result to 14 bit.

Common Measurement Settings
Settings common for the measurements, unless otherwise noted, is shown in Table 2. Descriptions of the measurement graphs are given in Table 3.

<table>
<thead>
<tr>
<th>Measurement Setup</th>
<th>Setting</th>
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<tbody>
<tr>
<td>ADC Supply</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Temperature</td>
<td>27 °C</td>
</tr>
<tr>
<td>LVDS Mode</td>
<td>12 bit (high-speed mode), 14 bit, 16 bit or dual 8 bit (precision mode)</td>
</tr>
<tr>
<td>LVDS Drive</td>
<td>RSDS</td>
</tr>
<tr>
<td>Fin</td>
<td>70 MHz -1dBfs</td>
</tr>
<tr>
<td>Sampling frequency, FS</td>
<td>640 MSPS / 320 MSPS / 160 MSPS (1 / 2 / 4 channel high-speed mode), 80MSPS / 105 MSPS (precision mode)</td>
</tr>
<tr>
<td>Jitter Control</td>
<td>8</td>
</tr>
</tbody>
</table>

Table 3: Graph descriptions used in the figures

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Description</th>
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<tbody>
<tr>
<td>0%</td>
<td>Bias Control set to normal</td>
</tr>
<tr>
<td>-20%</td>
<td>20% reduced Bias Current</td>
</tr>
<tr>
<td>-40%</td>
<td>40% reduced Bias Current</td>
</tr>
<tr>
<td>Raw</td>
<td>Direct output of ADC</td>
</tr>
<tr>
<td>Comp</td>
<td>Gain Mismatch, Time Skew and Offset Compensated Output</td>
</tr>
<tr>
<td>1x</td>
<td>1x gain (default)</td>
</tr>
<tr>
<td>2x</td>
<td>2x gain set in digital gain</td>
</tr>
</tbody>
</table>
Dynamic performance

Fin Sweep
The performance of the HMCAD1520 is measured in single, dual and quad channel mode at the sampling speed, FS, of 640 MSPS, 320 MSPS and 160 MSPS respectively. The performance is also measured in precision mode at the sampling speed, FS, of 80 MSPS and 105 MSPS.

Single Channel Mode, FS = 640 MSPS

Figure 4: SNR vs Fin

Figure 5: SNDR vs Fin

Figure 6: SFDR vs Fin

Figure 7: HD2 vs Fin

Figure 8: HD3 vs Fin
Dual Channel Mode, FS = 320 MSPS

**Figure 9: SNR vs Fin**

**Figure 10: SNDR vs Fin**

**Figure 11: SFDR vs Fin**

**Figure 12: HD2 vs Fin**

**Figure 13: HD3 vs Fin**
Quad Channel Mode, FS = 160 MSPS

Figure 14: SNR vs Fin

Figure 15: SNDR vs Fin

Figure 16: SFDR vs Fin

Figure 17: HD2 vs Fin

Figure 18: HD3 vs Fin
Precision Mode, FS = 80 MSPS and 105 MSPS

Figure 19: SNR vs Fin

Figure 20: SNDR vs Fin

Figure 21: SFDR vs Fin

Figure 22: HD2 vs Fin

Figure 23: HD3 vs Fin
FS Sweep
The performance of the HMCAD1520 is measured in single, dual and quad channel high-speed mode and precision mode.

Single Channel Mode, Fin = 70 MHz

Figure 24: SNR vs FS

Figure 25: SNDR vs FS

Figure 26: SFDR vs FS

Figure 27: HD2 vs FS

Figure 28: HD3 vs FS
Dual Channel Mode, Fin = 70 MHz

**Figure 29: SNR vs FS**

**Figure 30: SNDR vs FS**

**Figure 31: SFDR vs FS**

**Figure 32: HD2 vs FS**

**Figure 33: HD3 vs FS**
Quad Channel Mode, \( \text{Fin} = 70 \text{ MHz} \)

**Figure 34: SNR vs FS**

**Figure 35: SNDR vs FS**

**Figure 36: SFDR vs FS**

**Figure 37: HD2 vs FS**

**Figure 38: HD3 vs FS**
Precision Mode, \( F_{in} = 21 \text{ MHz}, 70 \text{ MHz} \) and 140 MHz

**Figure 39:** SNR vs FS

**Figure 40:** SNDR vs FS

**Figure 41:** SFDR vs FS

**Figure 42:** HD2 vs FS

**Figure 43:** HD3 vs FS
Vcm Sweep
The performance of the HMCAD1520 is measured in single, dual and quad channel high-speed mode. The input clock frequency is 640 MHz and the sampling frequency, FS, is internally divided to 640 MSPS, 320 MSPS and 160 MSPS respectively. The performance is also measured in precision mode at the sampling speed, FS, of 80 MSPS and 105 MSPS. The common mode voltage is swept from ~0.2 V to VDD-0.2 V.

Single Channel Mode, Fin = 70 MHz, FS = 640 MSPS

Figure 44: SNDR vs Vcm

Figure 45: SFDR vs Vcm

Dual Channel Mode, Fin = 70 MHz, FS = 320 MSPS

Figure 46: SNDR vs Vcm

Figure 47: SFDR vs Vcm

Quad Channel Mode, Fin = 70 MHz, FS = 160 MSPS

Figure 48: SNDR vs Vcm

Figure 49: SFDR vs Vcm
Precision Mode, \( F_{\text{in}} = 70 \text{ MHz}, \) \( F_S = 80 \text{ MSPS} \) and \( 105 \text{ MSPS} \)

![Figure 50: SNDR vs Vcm](image)

![Figure 51: SFDR vs Vcm](image)
Bias Control Setting
The performance of the HMCAD1520 is measured in single channel high-speed mode and precision mode for different bias control settings. The internal bias control settings are adjusted to 0% (normal setting), 20% and 40% reduced bias current.

Single Channel Mode, Fin = 70 MHz

![SNDR vs FS, for two Bias Settings](figure52)

![SFDR vs FS, for two Bias Settings](figure53)

Single Channel Mode, FS = 640 MSPS

![SNDR vs Fin, for three Bias Settings](figure54)

![SFDR vs Fin, for three Bias Settings](figure55)

Precision Mode, Fin = 70 MHz

![SNDR vs FS, for two Bias Settings](figure56)

![SFDR vs FS, for two Bias Settings](figure57)
**Digital Gain Setting**

The HMCAD1520 has an internal digital gain feature. Utilizing this feature the ADC can adapt to different input levels.

**Single Channel Mode, Fin = 70 MHz**

![SNDR vs FS](image1)

*Figure 58: SNDR vs FS*

![SFDR vs FS](image2)

*Figure 59: SFDR vs FS*
Input Power Level
The HMCAD1520 has been measured with -1 dBfs and -20 dBfs output signal range. The performance is measured in Precision Mode with Fin = 21 and 70 MHz.

Precision Mode

Figure 60: SNR [dBfs] vs FS

Figure 61: SNR [dBc] vs FS

Figure 62: SNDR vs FS

Figure 63: SFDR vs FS
Temperature Sweep
The performance of the HMCAD1520 is measured in single channel high-speed mode with a sampling frequency, FS, of 640 MSPS and in precision mode with a sampling frequency, FS, of 105 MSPS. The measurements are done at 1.8 V. The internal bias control settings are adjusted to normal bias current.

Single Channel Mode, \( F_{in} = 70 \, \text{MHz} \)

\[ \text{Figure 64: SNDR vs Temperature @ 1.8 V} \quad \text{Figure 65: SFDR vs Temperature @ 1.8 V} \]

Precision Mode, \( F_{in} = 70 \, \text{MHz} \)

\[ \text{Figure 66: SNDR vs Temperature @ 1.8 V} \quad \text{Figure 67: SFDR vs Temperature @ 1.8 V} \]
Supply Sweep
The performance of the HMCAD1520 is measured in single, dual and quad channel high-speed mode. The input clock frequency is 640 MHz and the sampling frequency, FS, is internally divided to 640 MSPS, 320 MSPS and 160 MSPS respectively. The performance is also measured in precision mode at the sampling speed, FS, of 80 MSPS and 105 MSPS. The ADC power supply is swept from 1.7 V to 2.0 V. The bias control settings are also set to normal and 40% reduced bias current.

Single Channel Mode, Fin = 70 MHz, FS = 640 MSPS

Dual Channel Mode, Fin = 70 MHz, FS = 320 MSPS

![Figure 68: SNDR vs Vdd (ADC supply)](image1)

![Figure 69: SFDR vs Vdd (ADC supply)](image2)

![Figure 70: SNDR vs Vdd (ADC supply)](image3)

![Figure 71: SFDR vs Vdd (ADC supply)](image4)
**Quad Channel Mode, Fin = 70 MHz, FS = 160 MSPS**

![SNDR vs Vdd (ADC supply)](image1)

*Figure 72: SNDR vs Vdd (ADC supply)*

![SFDR vs Vdd (ADC supply)](image2)

*Figure 73: SFDR vs Vdd (ADC supply)*

**Precision Mode, Fin = 70 MHz, FS = 80 MSPS and 105 MSPS**

![SNDR vs Vdd (ADC supply)](image3)

*Figure 74: SNDR vs Vdd (ADC supply)*

![SFDR vs Vdd (ADC supply)](image4)

*Figure 75: SFDR vs Vdd (ADC supply)*
Clock Jitter Control
The HMCAD1520 has an internal clock jitter control feature. The jitter control settings allows the user to set a trade-off between power consumption and clock jitter. The clock jitter depends on the number of bits set to ‘1’ in the jitter control register.

The sampling frequency, FS, is set to 640 MSPS and the input frequency, Fin, is set to 125 MHz and 250 MHz respectively. The number of bits that are set to “1” in the clock jitter register is then stepped from 1 to 8. 5 measurements at each jitter control setting is done. The results are an average of these measurements.

Single Channel High Speed Mode, FS = 640 MSPS

![Figure 76: SNR vs JitterCtrl](image)

Figure 76: SNR vs JitterCtrl
**Common Mode Buffer**
The common mode buffer in the ADC has 4 different settings: 'off', '±20', '±400' and '±700'. The two highest buffer drive strength is shown in Figure 77.

![Figure 77: Vcm buffer drive strength in '±400' and '±700' settings](image-url)
**Power consumption**

The power consumption of the HMCAD1520 is measured in single, dual and quad channel high-speed mode. The input clock frequency is 70 MHz (-1 dBfs) and the sampling frequency, FS, is internally divided to 640 MSPS, 320 MSPS and 160 MSPS respectively. The power consumption is also measured in precision mode at the sampling speed, FS, of 80 MSPS and 105 MSPS.

The ADC power supply is 1.8 V, the LVDS drive is set to RSDS, all input channels are “on” and the bias control settings are set to normal, 20% and 40% reduced bias current.

<table>
<thead>
<tr>
<th>Single Channel Mode, FS = 640 MSPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>BiasCtrl</td>
</tr>
<tr>
<td>Normal</td>
</tr>
<tr>
<td>-20%</td>
</tr>
<tr>
<td>-40%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Dual Channel Mode, FS = 320 MSPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>BiasCtrl</td>
</tr>
<tr>
<td>Normal</td>
</tr>
<tr>
<td>-20%</td>
</tr>
<tr>
<td>-40%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Quad Channel Mode, FS = 160 MSPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>BiasCtrl</td>
</tr>
<tr>
<td>Normal</td>
</tr>
<tr>
<td>-20%</td>
</tr>
<tr>
<td>-40%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Precision Mode, FS = 105 MSPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>BiasCtrl</td>
</tr>
<tr>
<td>Normal</td>
</tr>
<tr>
<td>-20%</td>
</tr>
<tr>
<td>-40%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Precision Mode, FS = 80 MSPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>BiasCtrl</td>
</tr>
<tr>
<td>Normal</td>
</tr>
<tr>
<td>-20%</td>
</tr>
<tr>
<td>-40%</td>
</tr>
</tbody>
</table>
**Time Skew Mismatch**

The time skew was measured in single channel mode with an input frequency, $F_{in}$, of 203.75 MHz and a clock frequency, $F_S$, of 500 MSPS. 5 chips are then measured 10 times each. The average time skew and standard deviation is then calculated.

Channel 1 is used as reference, and it therefore always is given as 0 ps time skew.

**Single Channel Mode, $F_S = 500$ MSPS**

<table>
<thead>
<tr>
<th>Channel</th>
<th>Average Time Skew [ps]</th>
<th>Standard Deviation [ps]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel 1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Channel 2</td>
<td>0.73</td>
<td>2.37</td>
</tr>
<tr>
<td>Channel 3</td>
<td>-0.31</td>
<td>1.42</td>
</tr>
<tr>
<td>Channel 4</td>
<td>3.22</td>
<td>1.54</td>
</tr>
<tr>
<td>Channel 5</td>
<td>4.82</td>
<td>2.21</td>
</tr>
<tr>
<td>Channel 6</td>
<td>1.52</td>
<td>0.94</td>
</tr>
<tr>
<td>Channel 7</td>
<td>3.57</td>
<td>2.62</td>
</tr>
<tr>
<td>Channel 8</td>
<td>4.06</td>
<td>1.58</td>
</tr>
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## Document Information

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