

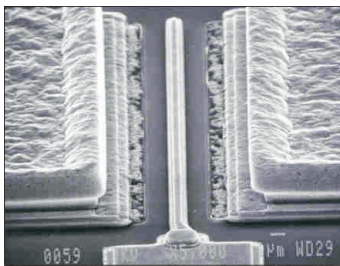


# Space Level (Class S) Product Screening

# SPACE

## Space Level (Class S) MMIC Die Screening & Qualification

Hittite Microwave offers Class S element evaluation in accordance with MIL-PRF-38534 on standard & custom product die. We are qualified by major spacecraft OEMs worldwide, shipping tens of thousands of S-Level MMICs which are currently operational on dozens of commercial, scientific & military spacecraft.



**FET Channel SEM**

Screening individual wafer lots is done to meet MIL-STD-883 Method 5007 wafer lot acceptance requirements. See "Wafer Acceptance Flow for Space Qualified MMICs" and table 2 "Class S & B MMIC Die/Wafer Screening & Qualification Procedure" herein. Measurements of internal wafer metal thickness and overall wafer thickness is done post wafer front & backside processing. A SEM analysis report per MIL-STD-883 method 2018 is completed and included in a final Wafer Acceptance report.

Hittite Microwave recommends 100% RF & DC testing on all deliverable flight hardware (wafer probe). This data will be delivered in print and/or electronic format to the customer. Software controlled test stands allow for S-parameter, spectrum related and large signal data to be collected over specific customer frequencies. This data will be presented to the customer in an aggregate form at the time the flight hardware is delivered. Serialized RF & DC data is also available upon request on same die process.

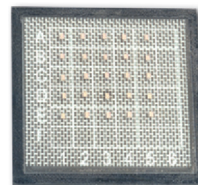
Hittite Microwave conducts 100% RF Probe on wafer test (DC - 110 GHz) and visual inspection in a class 100 environment per MIL-STD-883 Method 2010A utilizing laminar flow hoods in the production test and inspection areas. Die are shipped per customer request in either conductive standard waffle-packs or conductive standard Gel-Paks.

The LAT Process Flow for Space Qualified MMIC Die is shown herein. LAT includes High Temperature Operating Life (HTOL) testing which is performed at Hittite Microwave

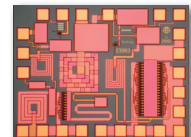


**Class 100 Visual Inspection & Test Area**

on the deliverable wafer lot. Samples from each wafer are subjected to a biased burn-in followed by a biased life test at elevated temperatures. This test simulates million hours of equivalent life at normal operating temperatures. Tests are conducted with DC bias to the MMIC device, which is closely monitored during the life test. Pre and Post-HTOL test delta limits are set up and measured on critical RF & DC parameters. The results are reported in the final LAT report.



**Serialized Die  
Delivered in GEL-PAK**



**InGaP HBT  
MMIC**



# Space Level (Class S) Product Screening

# SPACE

## Space Level (Class S) MMIC Die Screening & Qualification (Continued)

Sub Group	Class		Test	MIL-STD-883		Quantity (accept number)
	S	B		Method	Condition	
1	x	x	Element electrical			100 percent
2	x	x	Element visual	2010	A = Class S B = Class B	100 percent
3	x	x	Internal visual	2010	A = Class S B = Class B	10 (0)
4	x		Temperature cycling	1010	C	10 (0)
	x		Interim electrical			
	x		Burn-in	1015	240 hours minimum at +125°C, biased	
	x		Post burn-in electrical			
	x		Steady-state life	1005	1000 hours minimum at +125°C, biased	
	x	x	Final electrical			
5	x	x	Wire bond evaluation	2011	D	10 (0) wires or 20 (1) wires
6	x		Wafer Lot Acceptance Test (LAT) <ul style="list-style-type: none"> <li>SEM</li> <li>Wafer Thickness</li> <li>Metal Thickness</li> <li>Glassivation Thickness</li> </ul>	5007		5 (0) die per wafer

**Table 2:** Class S & B MMIC Die/Wafer Screening & Qualification Procedure